GT34TS02

Temperature Sensor

With 2Kb SPD EEPROM

Table of Content

1 Description

The GT34TS02 is a new Temperature Sensor (TS) product with embedded 2K-bit Serial Presence Detect (SPD) EEPROM, which is fully compatible to industrial standard I^2C™/SMBus interface and compliant to the JEDEC 42.4 specification. The EEPROM memory is organized as 256 x 8 bits and is functionally identical to the GT34C02. This new product is designed for memory module applications in most PC and Server platforms, as well as other related applications.

The unique GT34TS02 product operates from 2.7V to 3.6V and is offered in 8-pin Ultra-thin DFN package, 2 mm x 3 mm x 0.6 mm (max.), which is lead-free, RoHS, halogen free or Green compliance, providing space as well as cost saving for DIMM manufactures.

Temperature Sensor (TS)

The TS monitors the ambient temperature ranging from -40°C to 125°C. The TS includes a high precision CMOS temperature sensor, a sigma-delta analog to digital converter (ADC) and a serial interface compatible to industrial standard I^2C™/SMBus. The ADC default resolution is set at 12-bit (0.0625°C). The accuracy over various temperature ranges is:

- ±1°C (max) for temperature range from +70°C to +95°C
- ±2°C (max) for temperature range from +40°C to +125°
- ±3°C (max) for temperature range from -40°C to 125°C

The TS has shutdown current 5 μA (max.) with SPD EE in Standby mode.

The TS component has user-programmable registers that provide the capabilities for DIMM temperature-sensing applications. The open drain $\overline{\text{EVENT}}$ output pin is active when the monitoring temperature exceeds a programmable limit, or falls below or rises above an alarm window. The user has the option to set the $\overline{\text{EVENT}}$ output as a critical temperature output. This output can be configured to operate in either a comparator mode for thermostat operation or in interrupt mode.

2K-bit SPD EEPROM

The embedded 2K-bit serial SPD EEPROM has the functions identical to the GT34C02. One of the features is to permanently lock the data in its first half (lower) 128 bytes (address 00h to 7Fh). This feature is specifically designed for use in DRAM DIMM with SPD. All information concerning the DRAM module configuration (e.g. access speed, size, and organization) can be kept write-protected in the first half of the memory. The second half (upper) 128 bytes of the memory (address 80h to FFh) can also be write-protected using two different software write protection mechanisms. By sending a specified sequence to the device, the first 128 bytes memory can be write-protected either permanently or resettable. The operating ambient temperature ranging is from -40°C to +85°C.

2 Features

- Supply voltage: 2.7V to 3.6V
- 2-wire serial interface I^2C/SMBus compatible
- Speed up to 400 kHz
- Low operating current
  - 5 μA (max) TS in Shutdown mode and EEPROM in Standby
  - 200 μA (max) TS being active and EEPROM in Standby mode
  - 2 mA (max) TS in Shutdown and EEPROM are active
- Software Programmable Shutdown Mode
- Software reset feature

2.1 The 2Kb SPD EEPROM

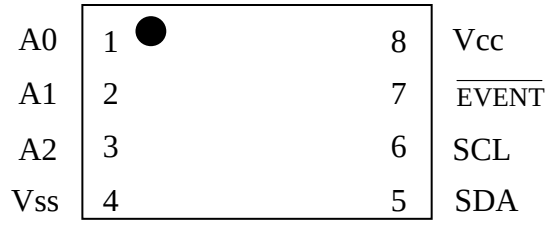
- Functionality identical to GT34C02 device
- Byte and Page (up to 16 bytes) Write Operations
- Random and Sequential Read modes
- Self-Time Write Cycle (5ms, max)
- Automatic Address Incrementing
- Permanent and Reversible Software data Protection for the lower 128 bytes
- Schmitt trigger on bus inputs
- Noise filter on bus inputs
- More than 1 million Erase/Write Endurance Cycles
- More than 40 years Data Retention
- Operating Temperature range: -40°C to +85°C

2.2 Temperature Sensor (TS)

- Temperature sensor accuracy (Grade B):
  - ±1°C from +70°C to +95°C
  - ±2°C from +40°C to +125°C
  - ±3°C from -40°C to +125°C
- Temperature sensor resolution: 0.0625°C/LSB
- The TS continuously monitors the temperature and updates the temperature data typically ten times per second. Temperature data is latched internally by the device and may be read by software from the bus host at any time.
- Temperature sampling (ADC conversion) time: 125 msec (max.)
- Hysteresis selectable set points from: 0, 1.5°C, 3°C & 6°C
- Ambient temperature sensing range: -40°C to +125°C

3 Pin Configuration

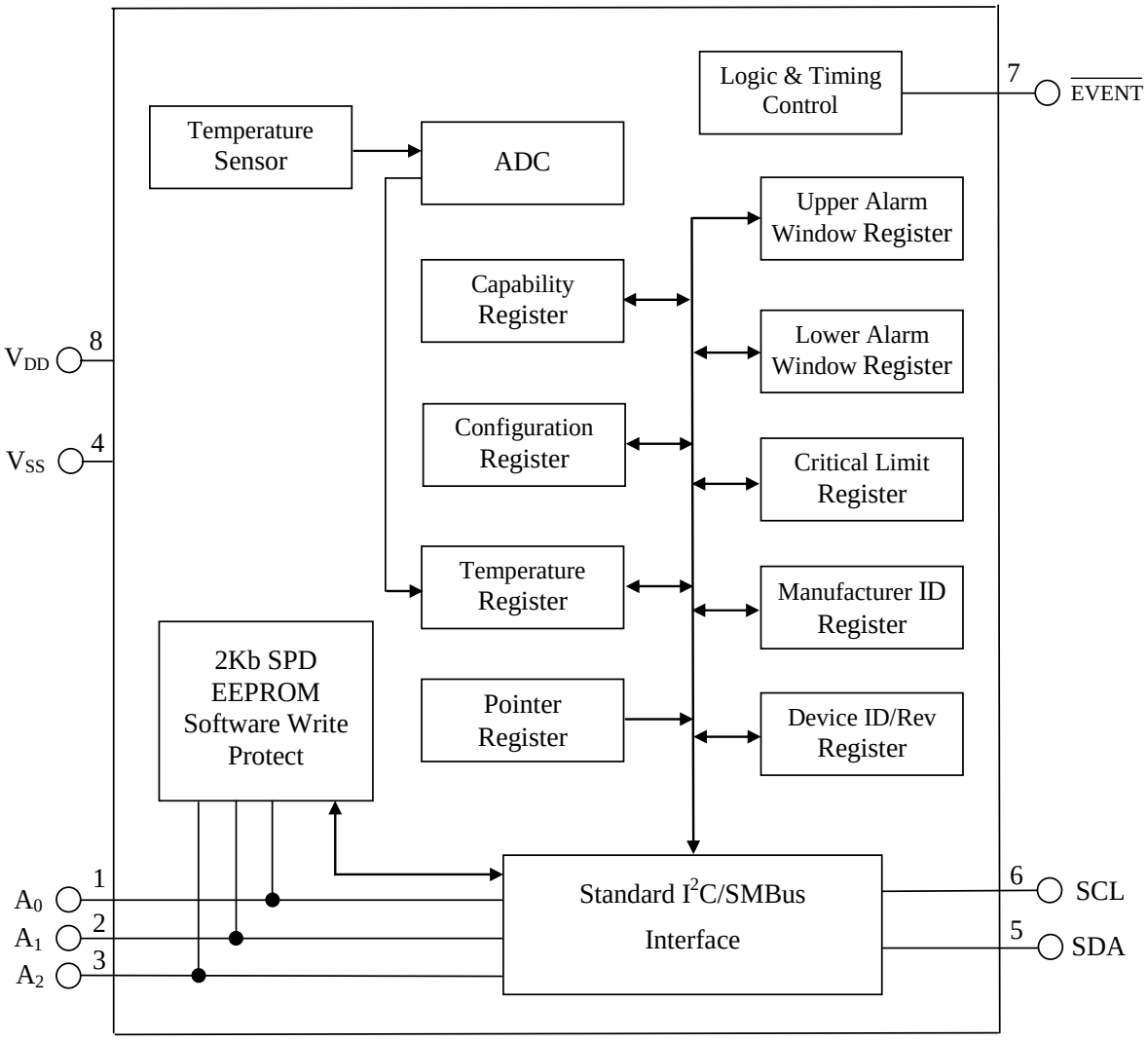
8-pin UDFN (top view)



Pin #	Symbol	Description	Type
1	A0	Device address selection pin	Input
2	A1	Device address selection pin	Input
3	A2	Device address selection pin	Input
4	V_{SS}	Ground	Ground
5	SDA	Serial Data (Open drain)	Input/Output
6	SCL	Serial clock	Input
7	$\overline{\text{EVENT}}$	$\overline{\text{EVENT}}$ pin (open drain and active-low) [1]	Output
8	V_{DD}	Supply voltage	Power

Note: [1] When active, functions as an Alert interrupt.

4 Block diagram



5 I²C / SMBus Serial Interface

5.1 Serial bus interface:

The GT34TS02 utilizes the industrial standard 2-wire bus supporting either I²C™ or SMBus protocol to communicate with a master controller. The master generates the SCL signal and GT34TS02 being a slave device utilizes the SCL signal to receive or send data via the SDA line. Data transfer is serial, bi-directional, and is one bit at a time with the Most Significant Bit (MSB) transferred first, and a complete I²C bus data is 1-byte. Since both SCL and SDA are open-drain, pull-up resistors are required.

5.2 Slave address:

GT34TS02 uses 7-bit slave address, which consists of 4 fixed bits (Device Type Identifier, D0~D3) and 3 programmable bits (A0, A1 and A2), allowing a total of eight devices to co-exist on the same bus. The input of each pin is sampled at the start of each I²C/SMBus access.

The TS and EEPROM in GT34TS02 each have its own unique I²C address for the 4 bits Device Type Identifier (DTI), which are the first 4 bits of the Slave address:

- 0011: TS
- 1010 : EE
- 0110: Access software write protection operations on the EEPROM

The rest of 3 bits, A2, A1 and A0, are configurable to select one of eight possible Slave devices.

The last bit, R/W, specifies whether a Read (1) or Write (0) operation is being performed.

Memory Area Function	Slave Address							
	Device Type Identifier				Select Address Signals			R/W#
	D3	D2	D1	D0	A2	A1	A0	
Read/Write TS registers	0	0	1	1	A2	A1	A0	R/W#
Read/Write EEPROM memory	1	0	1	0	A2	A1	A0	R/W#
Set Write Protection (SWP)	0	1	1	0	0	0	1	0
Clear Write Protection (CWP)					0	1	1	0
Permanently Set Write Protection (PSWP)					A2	A1	A0	0
Read SWP					0	0	1	1
Read CWP					0	1	1	1
Read PSWP					A2	A1	A0	1

Note: D3 (MSB), R/W# (LSB)

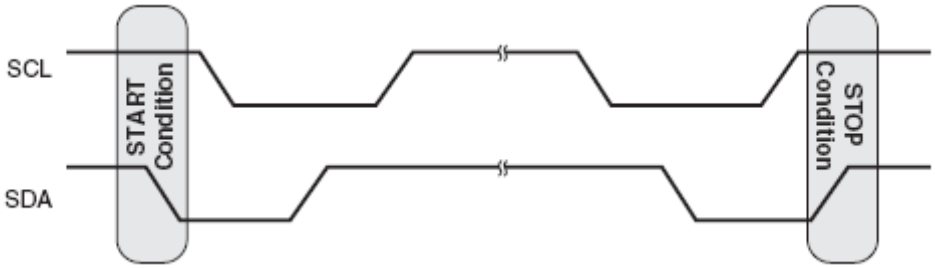
5.3 I²C / SMBus Communication

This protocol provides the communications to

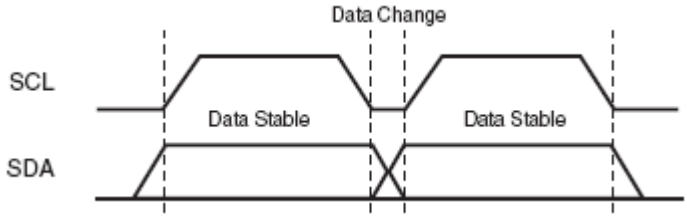
- The registers selected by the Pointer register.
- At power-up, the Pointer register is set to “00”, i.e. the Capability register location.
- The Pointer register latches the last location being set to. Also, pending upon the selected bits [P2:P0] of pointer register, each data registers falls into one of two types of user accessibility:
  - Read only
  - Write / Read

- A Write to GT34TS02 will always include the address byte and the pointer byte. A Write to any register other than the pointer register, requires two data bytes.
- A Read operation can be performed in either
  - If the location latched in the Pointer register is correct (most of the time it is expected that the Pointer register will point to one of the Read Temperature registers because that will be the data most frequently read), then the Read can simply consist of an address byte, followed by retrieval of the two data bytes, OR
  - If the Pointer register needs to be set, then an address byte, pointer byte, repeat start, and another address byte will accomplish a Read
- The data byte communication transfers the MSB (Bit 7) first.
- At the end of a Read, GT34TS02 can accept either an Acknowledge (ACK) or No Acknowledge (No ACK) status from the Master. The No ACK status is typically used as a signal for the slave that the Master has read its last byte. This device subsequently takes up to 125ms to measure the temperature.
- For the SMBus communication, conditions of 10kHz minimum clock frequency, 300ns data hold time and 50ms maximum time-out (TS only) are required.

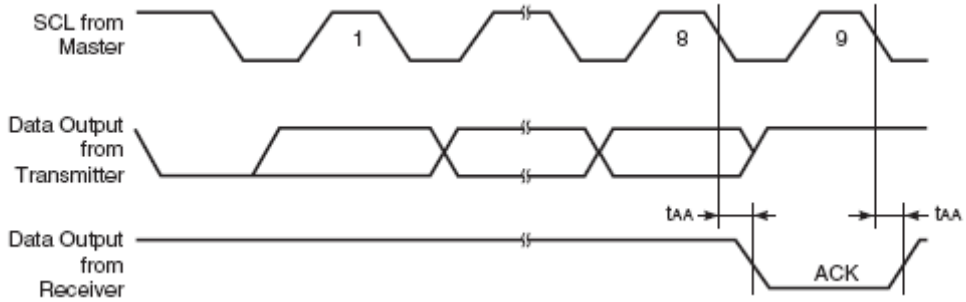
Start and Stop Conditions:



Data Validity Protocol:



Output Acknowledge:



6 Power-Up and Reset States

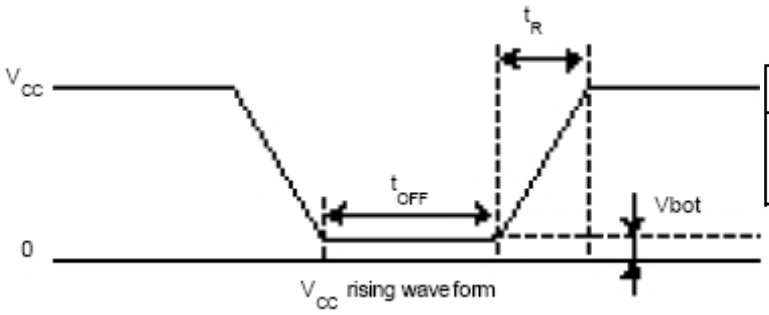
6.1 Power-Up Condition

After power-on, GT34TS02 is initialized to the following default condition:

- Pointer register is defaulted to 00h
- Starts monitoring local sensor
- $\overline{\text{EVENT}}$ register is cleared: $\overline{\text{EVENT}}$ output is pulled high by external pull-up resistor.
- $\overline{\text{EVENT}}$ hysteresis is defaulted to 0°C
- Critical temperature, Alarm Temperature Upper and Lower register are defaulted to 0°C
- Capability register is defaulted to 001Fh
- Operational mode: comparator
- After supply voltage reaches to a stable minimum level, TS needs a minimum of 250 msec prior to perform an appropriate measurement

6.2 Reset Condition

The device incorporates a power on reset circuit, which protects the internal logic against powering up into a wrong state. Nevertheless, the following conditions on power supply are recommended.



Tr	Toff	Vbot
Below 5ms	Above 10ms	Below 0.1V

7 Temperature Sensor (TS)

7.1 TS Register overview:

The TS component in GT34TS02 includes various types of user-programmable registers. Their definitions and functions are described in the following sections.

The major registers are:

- Pointer register
- Capability register
- Configuration register
- Upper Alarm Window register
- Lower Alarm Window register
- Critical Limit register
- Temperature register
- Manufacturer ID register
- Device ID/Revision register

Register Address	R/W	Default state	TS Register
N/A	W	N/A	Pointer register
00h	R	001Fh	Capability register (B-grade)
01h	R/W	0000h	Configuration register
02h	R/W	0000h	Upper Alarm Window register
03h	R/W	0000h	Lower Alarm Window register
04h	R/W	0000h	Critical Limit register
05h	R	N/A	Temperature register
06h	R	132Dh	Manufacturer ID register
07h	R	3300h	Device ID/Revision register

Note: Any illegal operations or write to invalid/reserved registers is prohibited.

7.1.1 Pointer register

This register is an 8 bits register, which contains 3 selected bits: P0, P1 and P2.

MSB			Pointer register				LSB
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	P2	P1	P0

Note: P2:P0 are selected bits of pointer register.

P2	P1	P0	Name	Description	R/W	Default
0	0	0	TSCap	TS capability	R	001F
0	0	1	Conf	Configuration	R/W	0000
0	1	0	Upper	Upper Alarm Window	R/W	0400
0	1	1	Lower	Lower Alarm Window	R/W	00A0
1	0	0	Critical	Critical Limit	R/W	0500
1	0	1	Temp	Temperature	R	0000
1	1	0	MID	Manufacturer ID	R	132Dh
1	1	1	DID	Device ID / Revision	R	3300h

7.1.2 Capability register

This register is a 16 bits register with default value 001Fh

MSB			Capability register (00h)				LSB
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
0	0	0	0	0	0	0	0
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RFU	RFU	RFU	Temperature resolution		Range	Accuracy	Alarm & Critical Trips
0	0	0	1	1	1	1	1

Bit	Symbol	R/W	Description
0	Alarm & Critical Trips	R	Basic capability. 0: The device does not support interrupt capabilities. 1 (Default): Has Alarm and Critical Trips capability
1	Accuracy	R	Higher accuracy bit set during manufacture. 0: Accuracy ±2°C over the active range and ±3°C over the monitor range (C-grade) 1 (Default): Accuracy ±1°C over the active range and ±2°C over the monitor range (B-grade)
2	Range	R	0: The temperature monitor clamps values lower than 0°C. 1 (Default): can be read temperatures below 0°C and set sign bit accordingly
4:3	Temperature resolution	R	Temperature resolution 11 (Default): This 12-bit setting provides temperature at 0.0625°C resolution (LSB)
15:5	RFU	R	Reserved for future use. Must be Zero

7.1.3 Configuration register

This register is a 16 bits register with default value 0000h

MSB			Configuration register (01h)				LSB
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
RFU	RFU	RFU	RFU	RFU	Hysteresis		Shutdown TS
0	0	0	0	0	0	0	0
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Critical Lock	$\overline{\text{EVENT}}$ Lock	Clear	$\overline{\text{EVENT}}$ Status	$\overline{\text{EVENT}}$ Control	Critical Event	$\overline{\text{EVENT}}$ Polarity	$\overline{\text{EVENT}}$ Mode
0	0	0	0	0	0	0	0

Bit	Parameter	R/W	Description
0	$\overline{\text{EVENT}}$ Mode	R/W	0: Comparator output mode (Default) 1: Interrupt mode • When either of the Alarm (6) or Critical (7) lock bit is set, this bit cannot be altered until unlocked
1	$\overline{\text{EVENT}}$ Polarity	R/W	0: Low (Default) 1: HIGH. • When either of the Alarm (6) or Critical (7) lock bit is set, this bit cannot be altered until unlocked.
2	Critical $\overline{\text{EVENT}}$	R/W	0: $\overline{\text{EVENT}}$ output on Alarm or Critical temperature event (Default) 1: $\overline{\text{EVENT}}$ only if temperature is above the value in the critical temperature register

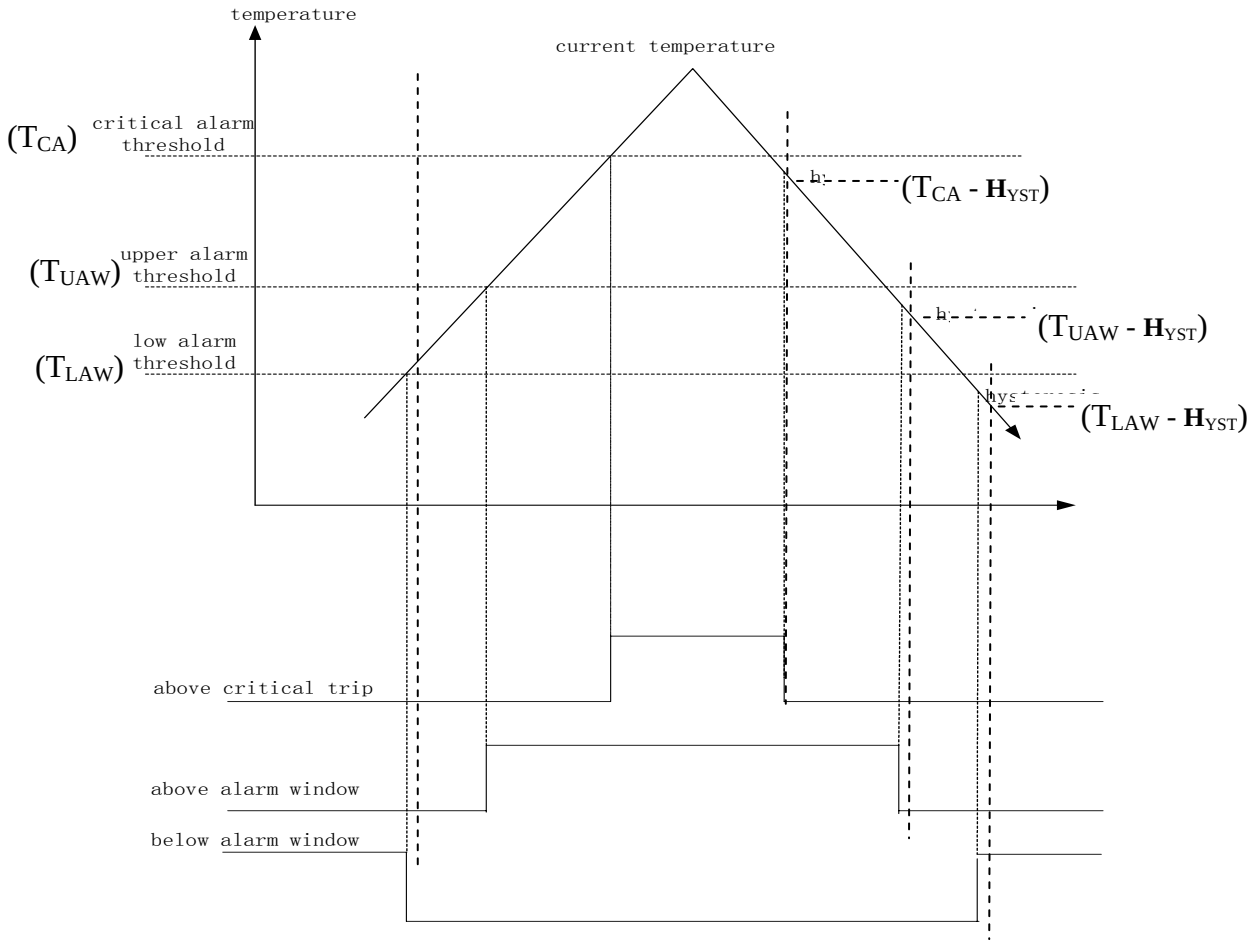
Bit	Parameter	R/W	Description
			• When the alarm window lock bit (6) is set, this bit cannot be altered until unlocked.
3	$\overline{\text{EVENT}}$ Control	R/W	0: $\overline{\text{EVENT}}$ output disabled (Default) 1: $\overline{\text{EVENT}}$ output enabled • When either of the lock bits (6 or 7) is set, this bit cannot be altered until unlocked.
4	$\overline{\text{EVENT}}$ Status	R	0: Not assert $\overline{\text{EVENT}}$ output condition (Default) 1: Assert $\overline{\text{EVENT}}$ output condition due to Alarm Window or Critical Trip condition. • The actual event causing the event can be determined from the Read Temperature register. Interrupt $\overline{\text{EVENT}}$ can be cleared by writing to the 'clear $\overline{\text{EVENT}}$' bit. Writing to this bit will have no effect
5	Clear	W	Clear $\overline{\text{EVENT}}$ 0: No-effect (Default) 1: Clears active $\overline{\text{EVENT}}$ in Interrupt mode. • When read, this register always returns zero. • Writing to this register has no effect in Comparator mode.
6	$\overline{\text{EVENT}}$ Lock	R/W	Alarm Window Lock bit 0: Upper and Lower Alarm Window registers are unlocked and can be altered (Default). 1: Upper and Lower Alarm Window registers are locked and setting cannot be altered. • Once power-up, this bit is initially cleared. When set, this bit will return a 1 and remains locked until cleared by internal power-on reset • This bit can be written with a single write and does not require double writes
7	Critical Lock	R/W	Critical Lock bit 0: Critical Limit register is unlocked and can be altered (Default) 1: Critical Limit register settings is locked and cannot be changed. • Once power-up, this bit is initially cleared. When set, this bit becomes a 1, and remains locked until cleared by internal Power-on reset • This bit can be written with a single write and do not require double writes.
8[1]	Shutdown TS	R/W	0: Enable TS (Default) 1: Disable TS • When disabled, entire TS component is shut down and enter into standby mode to save power, no events will be generated. However, all registers may be read or written to. • When either of the lock bits (6 or 7) is set, this bit cannot be set to 1 until they are unlocked. • However, this bit can be cleared to 0 at any time. Also, power cycling will clear this bit and enable the TS to active mode.
10:9	Hysteresis	R/W	00: Disable hysteresis (Default) 01: Enable hysteresis at 1.5°C 10: Enable hysteresis at 3°C 11: Enable hysteresis at 6°C • When enabled, hysteresis is applied to temperature movement around trigger points. Refer to Hysteresis section below for details.
15:11	RFU	R	Reserved for future use. Must be Zero

Notes:
[1] If either Bit 6 or Bit 7 is set, then this bit can't be set until they are unlocked.

Hysteresis is applied in the following conditions.

	Below Alarm window bit		Above Alarm window bit	
	Temperature slope	Threshold temperature	Temperature slope	Threshold temperature
Sets	Falling	T_{LAW} - $\mathbf{H}_{YST}$	Rising	T_{UAW}
Clears	Rising	T_{LAW}	Falling	T_{UAW} - $\mathbf{H}_{YST}$

Notes: T_{UAW} = Upper Alarm Window value; TLAW = Lower Alarm Window value; HYST = Absolute value of selected hysteresis; TCA = Critical Alarm value



- For example, consider the behavior of the 'Above Alarm Window' bit (bit 14) of the Temperature register with the hysteresis being set to 3 °C setting. As the ambient temperature rises and exceeds the alarm window, (i.e., when the Temperature register contains a value that is greater than the value of the Upper Alarm Window register), then bit 14 will be set to 1. If the ambient temperature decreases, bit 14 will remain set unless the measured temperature is less than or equal to 3°C below the value in the Upper Alarm Window register
- Similarly, the 'Below Alarm Window' bit (bit 13) of the Temperature register will be set to 0 when the value in the Temperature register is equal to or greater than the value in the Lower Alarm Window register. However, once the temperature decreases to less than the value in the Lower Alarm Window register minus 3°C, bit 13 will be set to 1.
- Note that hysteresis is also applied to $\overline{\text{EVENT}}$ pin functionality. When either of the lock bits (6 & 7) is set, these bits cannot be altered.

7.1.4 Temperature register

Bit	Symbol	Access	Description
12:0	TEMP	R	Temperature Value (2's complement). (LSB = 0.0625°C)

This register is a 16 bits register holding the temperature value

- The data of this register can be read at any time without interrupting the temperature conversion process
- The LSB (0) equals to 0.0625°C
- Bits 13 to 15 are limit setting bits

			MSB												LSB
Bit 15[*]	Bit 14[*]	Bit 13[*]	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Above Critical Alarm	Above Alarm Window	Below Alarm Window	Sign	Temperature value											0

Where [*] is

Bit #	Definition with Hysteresis = 0
13	Below Alarm Window • 0 : temperature is equal to or above the Lower Alarm Window register • 1 : temperature is below the Lower Alarm Window register When the temperature is below the Lower Alarm Window value, this bit is set and will remain set as long as the temperature is below the Lower Limit minus the hysteresis. When the temperature meets or exceeds the Lower Limit, it will only be cleared.
14	Above Alarm Window • 0 : temperature is equal to or below the Upper Alarm Window register • 1 : temperature is above Upper Alarm Window register When the temperature is above the Upper Alarm Window value, this bit is set and will remain set as long as the temperature is above the Upper value. Once when the temperature drops below or equal to the Upper value minus the hysteresis, it will be cleared.
15	Above Critical Alarm • 0 : temperature is below the Critical Alarm register setting • 1 : temperature is equal to or above the Critical Alarm register setting When the temperature is above the Critical Alarm, this bit is set and will remain set as long as the temperature is above Critical Alarm. Once the temperature has dropped below the limit minus the hysteresis, it will automatically be cleared.

7.1.5 Upper Alarm Window register

This register is a 16 bits register holding the Upper Alarm Window temperature value

- LSB equals to 0.25°C

			MSB											LSB	
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	Sign	Upper Alarm Window Temperature value										0	0

7.1.6 Lower Alarm Window Register

This register is a 16 bits register holding the Lower Alarm Window temperature value

- LSB equals to 0.25°C

			MSB											LSB		
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	Sign	Lower Alarm Window Temperature value										0	0

7.1.7 Critical Alarm register

This register is a 16 bits register holding the Critical Alarm temperature value

- LSB equals to 0.25°C

			MSB										LSB		
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	Sign	Critical Alarm Temperature value										0	0

7.1.8 Manufacturer's ID register

This register is a 16 bits register for Manufacturer ID (132Dh)

7.1.9 Device ID register

This register is a 16 bits register for Device ID (3300h)

- The upper byte stores a unique number Device ID.
- The lower byte holds the revision value.

7.2 $\overline{\text{EVENT}}$ *output:*

The $\overline{\text{EVENT}}$ pin is an open-drain output whose function can be programmed as an interrupt, comparator, or critical alarm mode.

7.2.1 Interrupt mode

- When the temperature exceeds the value in either the Upper or Lower Alarm Window register, the device will trigger the $\overline{\text{EVENT}}$ interrupt. By writing a "1" to the Clear $\overline{\text{EVENT}}$ bit (5) of Configuration Register will clear the status.

7.2.2 Comparator mode

- The $\overline{\text{EVENT}}$ pin remains asserted until the temperature falls below the value programmed in the Upper Alarm Window register or rises above the value programmed in the Lower Alarm Window register, or until the range of these alarm registers are reprogrammed and the temperature falls inside the Alarm limits.

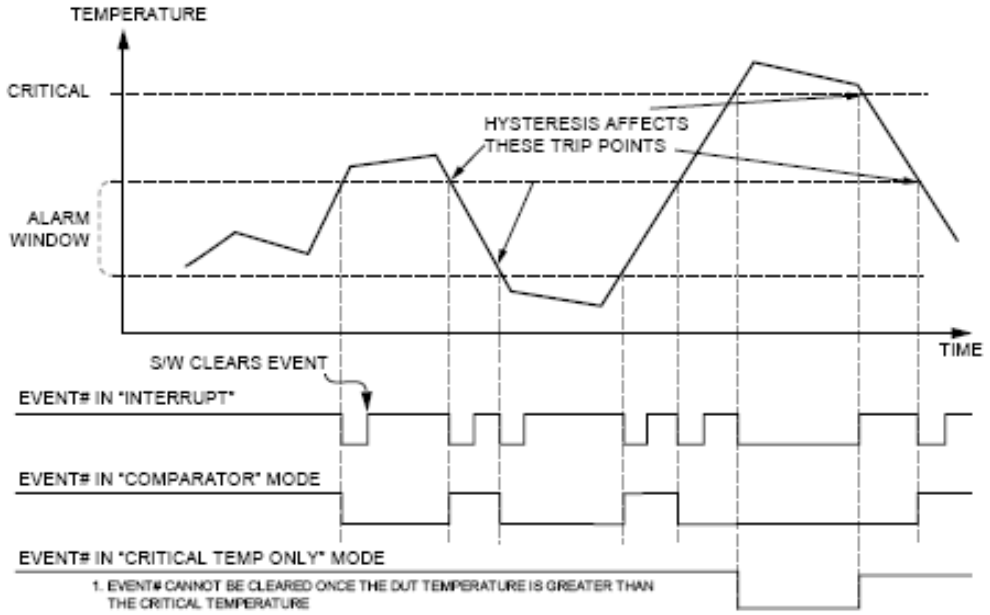
7.2.3 Critical mode

- When the temperature reaches beyond a critical temperature, the device switches to the comparator mode automatically and triggers the $\overline{\text{EVENT}}$ interrupt. Such state will remain as long as the temperature stays above the critical setting. Under such

condition, the $\overline{\text{EVENT}}$ Status cannot be cleared through the clear $\overline{\text{EVENT}}$ bit or SMBus Alert.

- When the temperature drops below critical temperature, the $\overline{\text{EVENT}}$ output can be only cleared and the device reverts back to either interrupt or comparator mode, pending upon the programmed status of Bit 0 ($\overline{\text{EVENT}}$ mode) in the Configuration register. Or performing the SMBus Alert Response address (ARA), if SMBus is utilized.

All event thresholds use hysteresis as programmed in the Configuration register.



7.3 Alarm window:

The alarm window consists of two registers: an Upper Alarm Window register (02h) and a Lower Alarm Window register (03h). The Upper Alarm Window register holds the upper temperature point, while the Lower Alarm Window register holds the lower temperature point. When the $\overline{\text{EVENT}}$ control is enabling, the $\overline{\text{EVENT}}$ output will be triggered whenever entering or exiting the alarm window.

8 EEPROM Functional Description

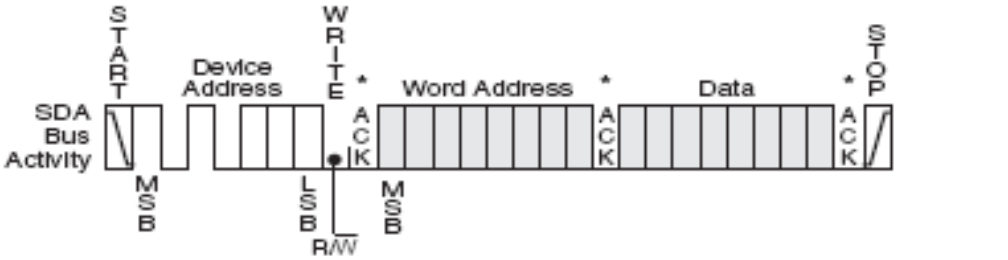
For EE, all functions on Read, Write, software protections and others are the same as GT34C02, which includes byte write, page write, random access read, current address read, sequential read, SWP, CWP and PSWP.

8.1 Command Configuration:

Pin Connection[1]			Slave Device Address								
A2	A1	A0	BIT	7	6	5	4	3	2	1	0	
A2	A1	A0		1	0	1	0	A2	A1	A0	R/$\overline{W}$	Normal Instruction[2]
A2	A1	A0		0	1	1	0	A2	A1	A0	R/$\overline{W}$	Permanent Write Protection Instruction[2]
GND	GND	V_{HV}		0	1	1	0	0	0	1	0	Set Write Protection (SWP)
GND	V_{CC}	V_{HV}		0	1	1	0	0	1	1	0	Clear Write Protection (CWP)
GND	GND	V_{HV}		0	1	1	0	0	0	1	1	Read SWP
GND	V_{CC}	V_{HV}		0	1	1	0	0	1	1	1	Read CWP

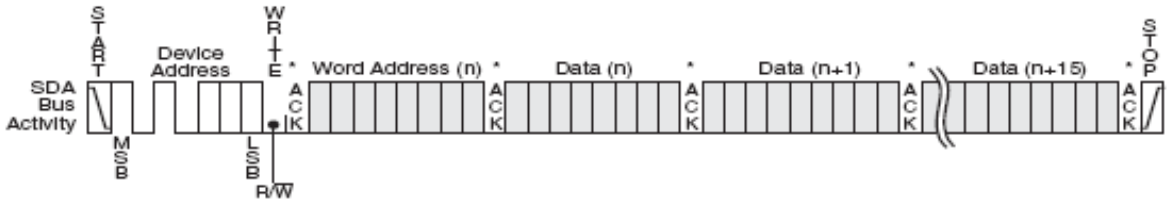
Note:
1. A2-A0 input pin connections must be GND (or floating), V_{CC}, or V_{HV}.
2. Bits 1, 2, and 3 of the device address will be compared with the values on the external pins.

8.2 Byte Write:



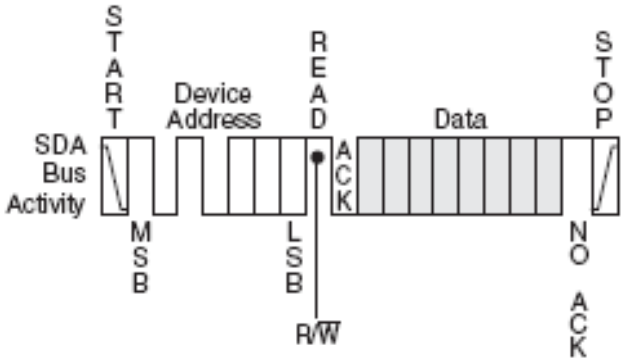
* Acknowledges provided by the slave regardless of hardware or software Write Protection.

8.3 Page Write:

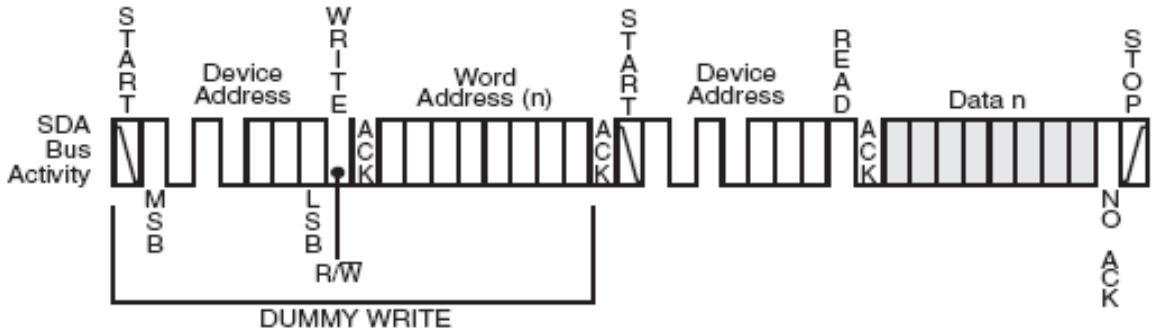


* Acknowledges provided by the slave regardless of hardware or software Write Protection.

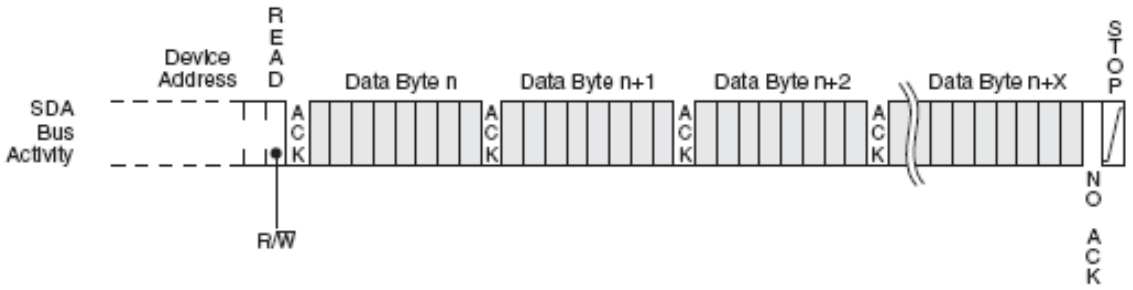
8.4 Current Address Read:



8.5 Random Address Read:



8.6 Sequential Read:



8.7 Software Write Protection:

The EEPROM has two software write-protection features, allowing the lower half of the memory area (addresses 0x00 to 0x7F) to be temporarily or permanently write protected. Software write-protection is handled by three instructions:

- SWP: Set Write Protection
- CWP: Clear Write Protection
- PSWP: Permanently Set Write Protection

The level of write-protection (set or cleared) that has been defined using these instructions, remains defined even after a power cycle.

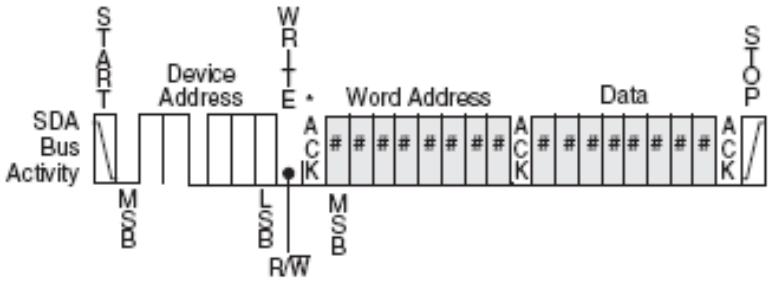
8.8 SWP and CWP:

If the software write-protection has been set with the SWP instruction, it can be cleared again with a CWP instruction.

The two instructions (SWP and CWP) have the same format as a Byte Write instruction, but with a different Device Type Identifier. Like the Byte Write instruction, it is followed by an address byte and a data byte, but in this case the contents are all “Don't Care”. Another difference is that the voltage, VHV must be applied on the A0 pin, and specific logical levels must be applied on the other two A1 pin and A2 pin.

8.9 PSWP:

If the software write-protection has been set with the PSWP instruction, the first 128 bytes of the memory are permanently write-protected. This write-protection cannot be cleared by any instruction, or by power-cycling the device. Also, once the PSWP instruction has been successfully executed, the SPD EE no longer acknowledges any instruction (with a Device Type Identifier of 0110) to access the write-protection settings.



* The slave does not provide an acknowledgement if the permanent write protection is already enabled.

Don't care bits are required.

8.10 Reading Write Protection Status:

The status of software write protection can be determined using these instructions:

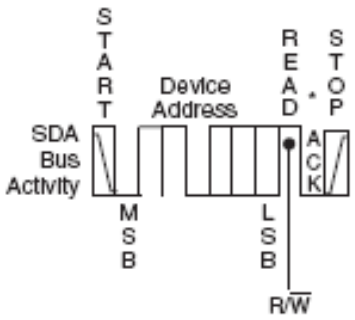
- Read SWP: Read Write Protection Status
- Read PSWP: Read Permanently Set Write Protection Status

8.11 Read SWP:

The host issues a Read SWP command. If Software Write Protection has not been set, the device replies to the data byte with an Ack. If Software Write Protection has been set, the device replies to the data byte with a NoAck.

8.12 Read PSWP:

The host issues a Read PSWP command. If Permanent Software Write Protection has not been set, the device replies to the data byte with an Ack. If Permanent Software Write Protection has been set, the device replies to the data byte with a NoAck.



* The slave does not provide an acknowledgement if the permanent write protection is already enabled.

9 Maximum Absolute Ratings

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{DD}	Supply voltage		-0.3	+4.2	V
V_n	Voltage on any other pin	SDA, SCL, $\overline{EVENT}$ pins	-0.3	+4.2	V
V_{A0}	Voltage on pin A0	Over voltage input; A0 pin	-0.3	+10	V
I_{sink}	Sink current	At SDA, SCL, $\overline{EVENT}$ pins	-1	+12.0	mA
$T_{j(max)}$	Maximum junction temperature			150	°C
T_{stg}	Storage temperature		-65	+150	°C

Notes:

Absolute maximum ratings are limits beyond which operation may cause permanent damage to the device. These are stress ratings only; functional operation at or above these limits are not implied.

10 DC Characteristics

V_{DD} = 2.7V to 3.6V, T_{amb} = -40 °C to +85 °C, unless otherwise specified

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage		2.7	3.3	3.6	V
I_{LIH} , I_{LIL} , I_{LOH} , I_{LOL}	Input/Output Leakage current	V_{PIN} = V_{DD} or V_{SS}			±4	μA
I_{CC1}	Operating current	TS active and EE standby			200	uA
I_{CC2}	Operating current	TS shutdown and EE active			2	mA
I_{SD}	Shutdown current	TS shutdown, EE standby (I^2C/SMBus inactive)			5	uA
V_{IH}	Input High Voltage	SCL, SDA	0.7* V_{DD}		V_{DD}+0.5	V
V_{IL}	Input Low Voltage	SCL, SDA	-0.5		0.3* V_{DD}	V
V_{HV}	A0 High Voltage	V_{HV} - V_{DD} ≥ 4.8V	7		10	V
V_{OL}	Output Low Voltage	I_{OL} =2.1mA, 2.7<= V_{DD} <=3.6			0.4	V
		I_{OL} =0.7mA, V_{DD} = 2.7			0.2	
$I_{OL\_\overline{EVENT}}$	Output Low Sink Current on $\overline{EVENT}$	V_{OL} = 0.4V	1			mA
I_{OL_SDA}	Output Low Sink Current on SDA	V_{OL} = 0.6V	6			mA
TS_{Acc}	Temperature sensor (TS) accuracy (B-grade)	T_{amb}= 70 °C to 95 °C			±1.0	°C
		T_{amb}= 40 °C to 125 °C			±2.0	°C
		T_{amb}= -40 °C to 125 °C			±3.0	°C
TS_{Res}	TS Resolution	12-bit ADC			0.0625	°C/LSB
R_{ADC}	ADC Resolution				12	Bits
TS_{Conv}	Conversion Rate				125	ms

Notes:

- Not all parameters are 100% tested.
- This specification only indicates how often temperature information is updated to the Temperature Register.
- Accuracy (express in °C) = difference between the output temperature and the measured temperature

Pin Impedance Characteristics

V_{DD} = 2.7V to 3.6V, T_{amb} = 25°C, unless otherwise specified

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
C_{IN1}	SDA, $\overline{EVENT}$ pin capacitance	Vin = 0			8	pF
C_{IN2}	Input capacitance (other pins)	Vin = 0			6	pF

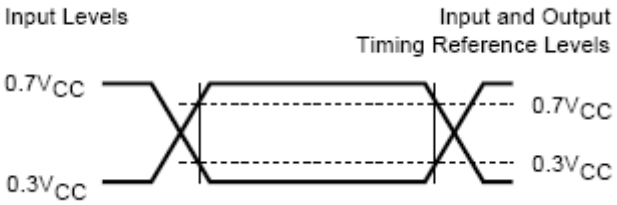
11 AC Characteristics

V_{DD} = 2.7V to 3.6V, T_{amb} = 25°C, unless otherwise specified

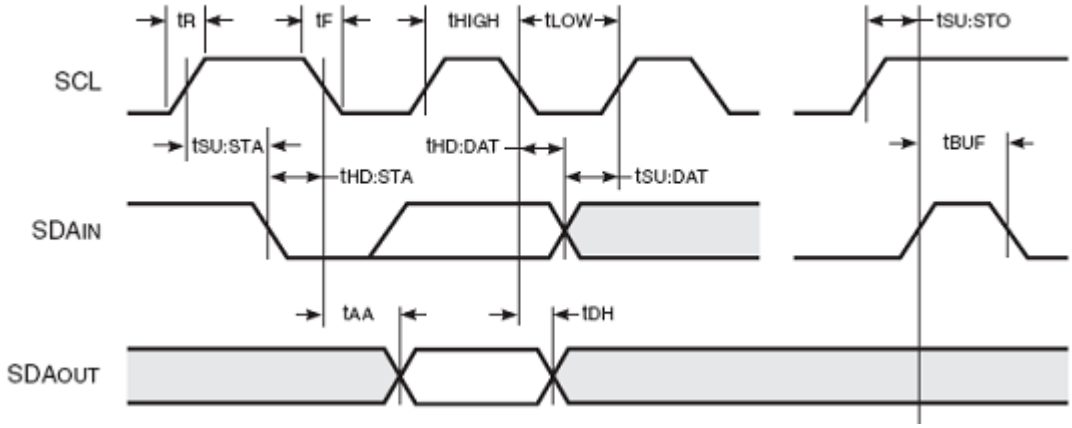
Symbol	Parameter [1]	Min.	Typ.	Max.	Unit
f_{SCL}	SCL clock frequency	10		400	kHz
t_{LOW}	Low period of SCL clock	1.3			µs
t_{HIGH}	High period of SCL clock	0.6			µs
t_{BUF}	Bus free time between a Stop and a Start conditions	1.3			µs
$t_{SU;STA}$	Start condition Setup time	600			ns
$t_{HD;STA}$	Start condition Hold time	0.6			µs
$t_{SU;STO}$	Stop condition Setup time	0.6			µs
$t_{SU;DAT}$	Data In Setup time	100			ns
$t_{HD;DAT}$ [2]	Data In Hold time	0			ns
t_{DH}	Data Out Hold Time	300		900	ns
t_{AA}	SCL Low to SDA Data Out	200		900	ns
t_{WR}	Write Cycle			5	ms
t_R	Rise time of SDA and SCL			300	ns
t_F	Fall time of SDA and SCL			300	ns
T	Noise Suppression time			100	ns
t_{PU} [3]	Power-up to temperature measurement	250			ms
$t_{time\text{-}out}$ [4]	Bus time-out (TS only)	20		50	ms

Notes:
[1] Not all parameters are 100% tested.
[2] For the SMBus, 300 ns data in hold time, $t_{HD;DAT}$, is required.
[3] After Vcc reaches the nominal value, 250msec is required prior to a valid temperature measurement
[4] The SMBus has a time-out of up to 50 ms for TS.

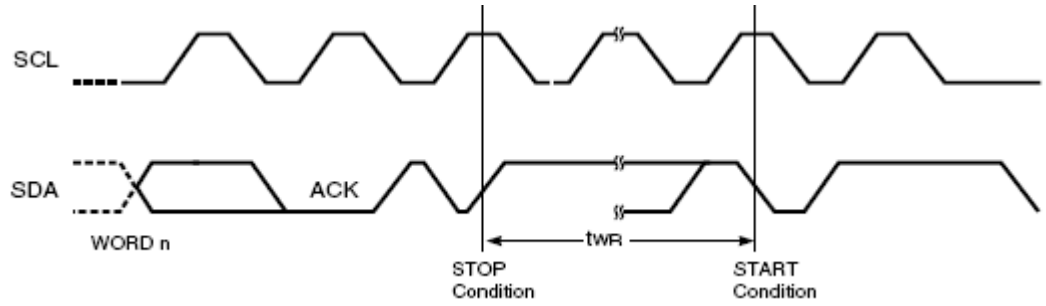
AC measurement I/O waveform



I²C / SMBus AC timing consideration:



Write cycle Timing:



12 Ordering Information

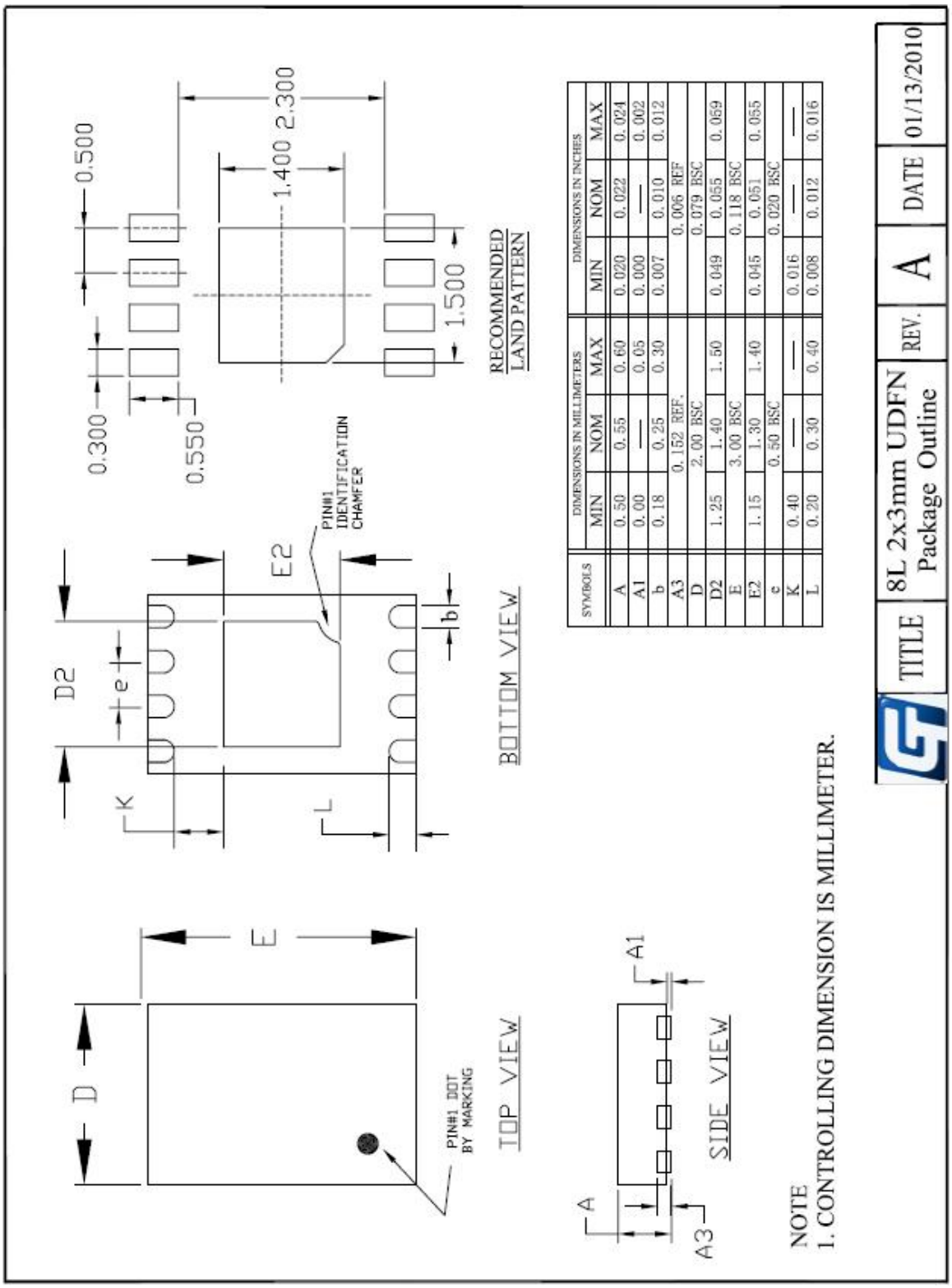
Voltage Range	Part Number	Package (8 Pins)
2.7V to 3.6V	GT34TS02-3UDLI-TR	Ultra-thin DFN 2 x 3 x 0.6 (max) mm

Note:

1. Contact Giantec Sales Representatives for availability and other information.
2. The UDFN is offered in T&R only in multiples of 5k.
3. Refer to Giantec website for related declaration document on lead free, RoHS, halogen free, or Green, whichever is applicable.

13 Package

Ultra-thin DFN (UDFN)



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.50	0.55	0.60	0.020	0.022	0.024
A1	0.00	—	0.05	0.000	—	0.002
b	0.18	0.25	0.30	0.007	0.010	0.012
A3		0.152 REF.			0.006 REF	
D		2.00 BSC			0.079 BSC	
D2	1.25	1.40	1.50	0.049	0.055	0.059
E		3.00 BSC			0.118 BSC	
E2	1.15	1.30	1.40	0.045	0.051	0.055
e		0.50 BSC			0.020 BSC	
K	0.40	—	—	0.016	—	—
L	0.20	0.30	0.40	0.008	0.012	0.016

14 REVISION HISTORY

Revision	Date	Descriptions
a0	Jan 2010	Initial draft