



**GT25A1024A**

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# **GT25A1024A**

**Automotive 1024-Kbit**

**SPI Bus**

**EEPROM**

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# GT25A1024A

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# GT25A1024A

## 1. Features

- Serial Peripheral Interface (SPI) Compatible
  - Supports Mode 0 (0,0) and Mode 3 (1,1)
- Wide-voltage Operation
  - $V_{CC} = 1.7V$  to  $5.5V$
- Operating Frequency:
  - 20 MHz for  $V_{CC} \geq 4.5V$
  - 10 MHz for  $V_{CC} \geq 2.5V$
  - 5 MHz for  $V_{CC} \geq 1.7V$
- Low power CMOS:
  - Standby current (max.):  $10\mu A$ , 5V
  - Operating current (max.): 5 mA, 5V
- Memory organization: 1024Kb (131072x 8)
- Page Size: 256 bytes
- Byte and Page write mode
  - Partial page writes allowed
  - Addition write lockable page
- Identification Page 128Bytes
- Block Write Protection
  - Protect 1/4, 1/2, or Entire Array
- Self-timed write cycle: 5 ms (max.)
- Endurance:
  - ✧ 4 million Write cycles at 25 °C
  - ✧ 1.2 million Write cycles at 85 °C
  - ✧ 600 k Write cycles at 125 °C
- Data retention
  - ✧ 50 years at 125 °C
  - ✧ 100 years at 25 °C
- Compliant with AEC-Q100 grade 1
- Packages: SOIC, TSSOP.
- ESD Protection  $\pm 8000V$
- Lead-free, RoHS, Halogen free, Green
- Noise immunity on inputs, besides Schmitt trigger

## 2. General Description

The GT25A1024A is a 1024Kbit serial EEPROM Automotive grade device operating up to 125 °C, which is compliant with the very high level of reliability defined by the automotive standard AEC-Q100 grade 1. The GT25A1024A utilizes standard Serial Peripheral Interface (SPI) for communications and contains a memory array of 1024K bits (131072 x 8), which is organized in 256 bytes per page.

The EEPROM operates in a wide voltage range from 1.7V to 5.5V running up to 20MHz, which fits most application. The product provides low-power operations and low standby current. The device is offered in Lead-free, RoHS, halogen free or Green package. The available package types are 8-pin SOIC, TSSOP.

This product has a compatible SPI interface: Chip-Select ( $\overline{CS}$ ), Serial Data In (SI), Serial Data Out (SO) and Serial Clock (SCK) for high-speed communication. Furthermore, a Hold feature via  $\overline{HOLD}$  pin allows the device entering into a suspended state whenever necessary and resuming the communication without re-initializing the serial sequence. A Status Register facilitates a flexible write protection mechanism and device status monitoring.

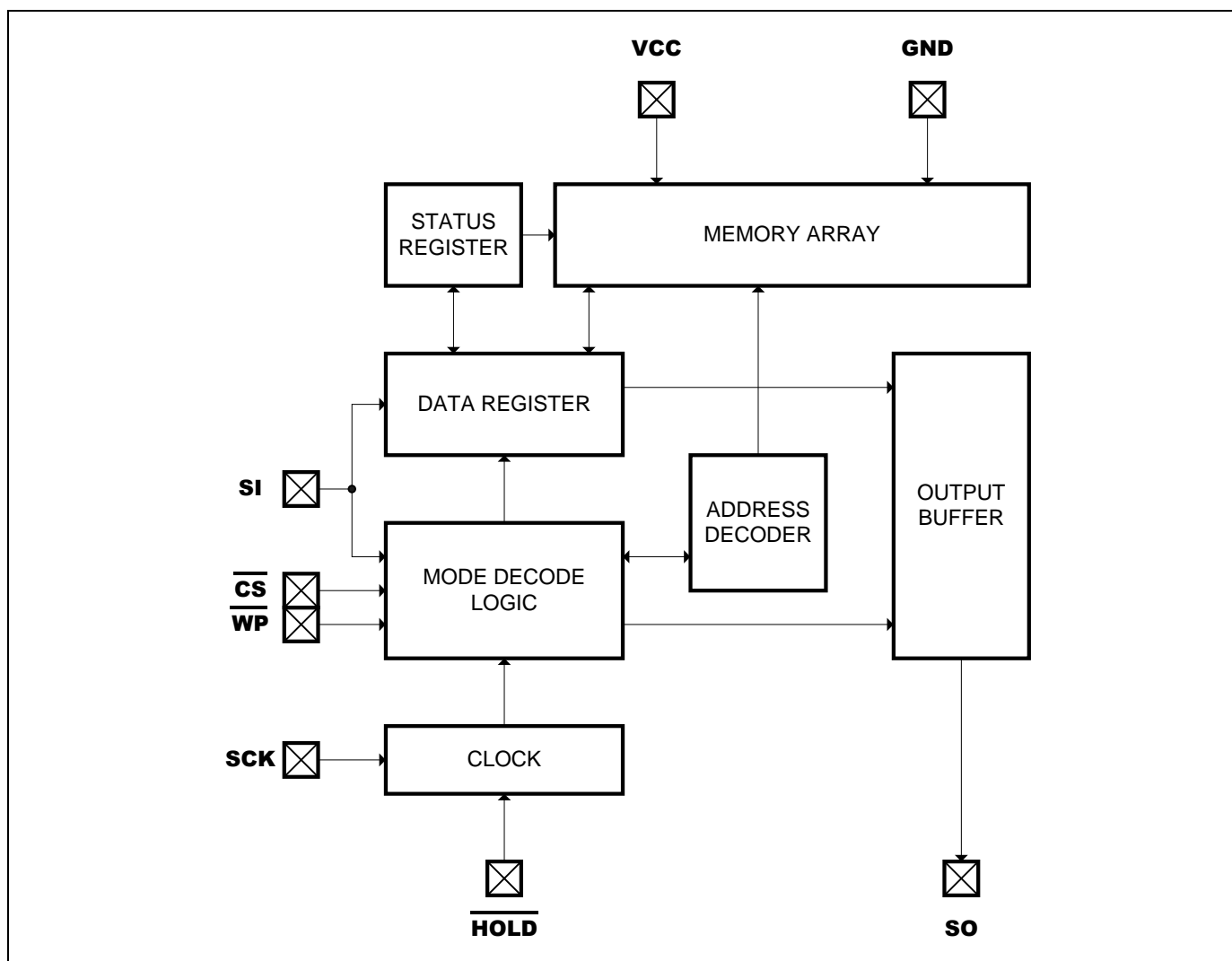
In order to refrain the state machine from entering into a wrong state during power-up sequence or a power toggle off-on condition, a power on reset circuit is implemented. During power-up, the device does not respond to any instructions until the supply voltage ( $V_{CC}$ ) has reached an acceptable stable level above the reset threshold voltage. Once  $V_{CC}$  passes the power on reset threshold, the device is reset and enters into the Standby mode. This should also avoid any inadvertent Write operations during power-up stage. During power-down process, the device will enter into standby mode, once  $V_{CC}$  drops below the power on reset threshold voltage. In addition, the device will be in standby mode after receiving the Stop command, provided that no internal write operation is in progress. Nevertheless, it is illegal to send a command unless the  $V_{CC}$  is within its operating level.

This product optionally offers an additional page (Identification Page) of 128 bytes. The Identification Page can be used to store sensitive application parameters which can be (later) permanently locked in Read-only mode.



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## 3. Functional Block Diagram



## Serial Interface Description

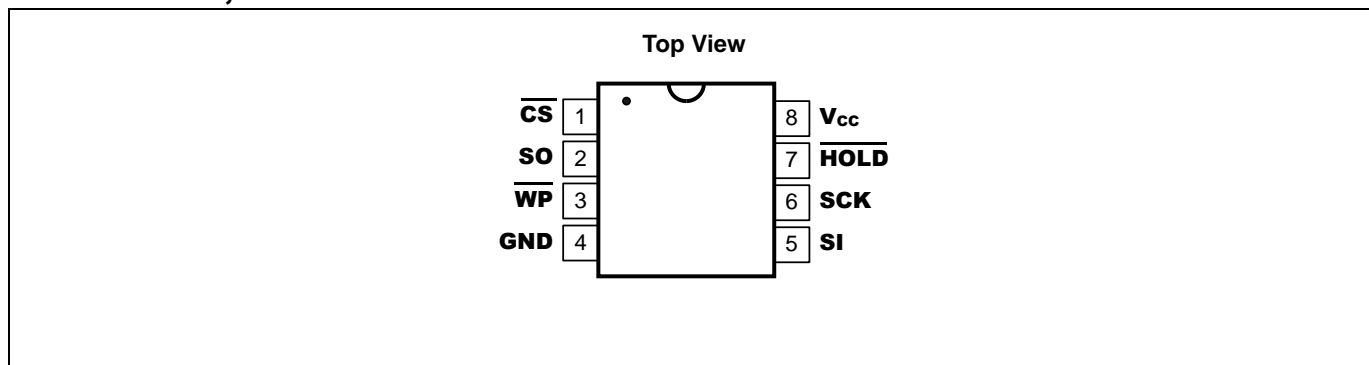
- Master:** The device that provides a clock signal.
- Slave:** GT25A1024A.
- Transmitter/Receiver:** The GT25A1024A has both data input (SI) and data output (SO).
- MSB** MSB (Most Significant Bit) is the first bit being transmitted or received.
- Op-Code:** Operational instruction code typically sent to the GT25A1024A is the first byte of information transmitted after  $\overline{\text{CS}}$  is Low. If the Op-Code is a valid instruction as listed in Table 5.4, then it will be decoded appropriately. It is prohibited to send an invalid Op-Code.



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## 4. Pin Configuration

### 4.1 8-Pin SOIC, TSSOP



### 4.2 Pin Definition

Pin No.	Pin Name	I/O	Definition
1	$\overline{CS}$	I	Chip Select
2	SO	O	Serial Data Output
3	$\overline{WP}$	I	Write Protect Input
4	GND	-	Ground
5	SI	I	Serial Data Input
6	SCK	I	Serial Clock
7	$\overline{HOLD}$	I	Hold function
8	V <sub>cc</sub>	-	Supply Voltage

### 4.3 Pin Descriptions

#### Chip Select ( $\overline{CS}$ )

The  $\overline{CS}$  pin is used to enable or disable the device. Upon power-up,  $\overline{CS}$  must follow the supply voltage. When the device is ready for instruction input, this signal requires a High-to-Low transition. Once  $\overline{CS}$  is stable at Low, the device is enabled. Then the master and slave can communicate among each other through SCK, SI, and SO pins. Upon completion of transmission,  $\overline{CS}$  must be driven to High in order to stop the operation or start the internal write operation. The device will enter into standby mode, unless an internal write operation is in progress. During this mode, SO becomes high impedance.

#### Serial Clock (SCK)

Under the SPI modes (0, 0) and (1, 1), this clock signal provides synchronization between the master and GT25A1024A. Typically, Op-Codes, addresses and data are latched from SI at the rising edge of SCK, while data from SO are clocked out at the falling edge of SCK.

#### Serial Data Input (SI)

Data Input pin.

#### Serial Data Output (SO)

Data output pin.



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## **Write Protect ( $\overline{\text{WP}}$ )**

This active Low input signal is utilized to initiate Hardware Write Protection mode. This mode prevents the Block Protection bits and the WPEN bit in the Status Register from being modified. To activate the Hardware Write Protection,  $\overline{\text{WP}}$  must be Low simultaneously when WPEN is set to 1.

## **Hold ( $\overline{\text{HOLD}}$ )**

This feature is used to suspend the device in the middle of a serial sequence and temporarily ignore further communication on the bus (SI, SO, SCK). The  $\overline{\text{HOLD}}$  signal transitions must occur only when SCK is Low and be held stable during SCK transitions. Connecting  $\overline{\text{HOLD}}$  to High disables this feature.

**Note:**  $\overline{\text{HOLD}}$  cannot be powered on earlier than Vcc, and the amplitude of  $\overline{\text{HOLD}}$  cannot be greater than Vcc.



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## 5. Device Operation

### 5.1 Status Register

The Status Register accessible by the user consists of 8-bits data for write protection control and write status. It becomes Read-Only under any of the following conditions: Hardware Write Protection is enabled or WEN is set to 0. If neither is true, it can be modified by a valid instruction.

**Table 5.1: Status Register**

Bit	Symbol	Name	Description
0	$\overline{\text{RDY}}$	Ready	When $\overline{\text{RDY}} = 0$ , device is ready for an instruction. When $\overline{\text{RDY}} = 1$ , device is busy. As busy, device only accepts Read Status Register command.
1	WEN	Write Enable	This represents the write protection status of the device. When WEN = 0, Status Register and entire array cannot be modified, regardless the setting of WPEN, $\overline{\text{WP}}$ pin or block protection. Write Enable command (WREN) can be used to set WEN to 1. Upon power-up stage, WEN is reset to 0.
2	BP0	Block Protect Bit	Despite of the status on WPEN, $\overline{\text{WP}}$ or WEN, BP0 and BP1 configure any combinations of the four blocks being protected (Table 5.2). They are non-volatile memory and programmed to 0 by factory.
3	BP1	Block Protect Bit	
4	X	Don't Care	
5	X	Don't Care	Values can be either 0 or 1, but are not retained. Mostly always 0, except during write operation.
6	X	Don't Care	
7	WPEN	Write Protect Enable	This bit can be utilized to enable Hardware Write Protection, together with $\overline{\text{WP}}$ pin. If enabled, Status Register becomes read-only. However, the memory array is not protected by this mode. Hardware Write Protection requires the setting of $\overline{\text{WP}} = 0$ and WPEN = 1. Otherwise, it is disabled. WPEN cannot be altered from 1 to 0 if $\overline{\text{WP}}$ is already set to Low. (Table 5.3 for write protection)

Note:

- 1, During internal write cycles, bits 0 to bit 7 are temporarily 1's.
- 2, After performing the write operation, the Ready bit may appear at any position from bit 0 to bit 7 when it first changes from 1b to 0b. When reading this result, Master needs to read the register again to read the correct value.
- 3, The method of delaying reading the register by 5ms after the write operation is also recommended.

**Table 5.2: Block Protection by BP0 and BP1**

Level	Status Register Bits		Array Addresses Protected
	BP1	BP0	
0	0	0	None
1 (1/4)	0	1	18000h-1FFFFh
2 (1/2)	1	0	10000h-1FFFFh
3 (All)	1	1	00000h-1FFFFh



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**Table 5.3: Write Protection**

WPEN	$\overline{WP}$	Hardware Write Protection	WEN	Inside Block	Outside Block	Status Register (WPEN, BP1, BP0)
0	X	Not Enabled	0	Read-only	Read-only	Read-only
0	X	Not Enabled	1	Read-only	Unprotected	Unprotected
1	0	Enabled	0	Read-only	Read-only	Read-only
1	0	Enabled	1	Read-only	Unprotected	Read-only
X	1	Not Enabled	0	Read-only	Read-only	Read-only
X	1	Not Enabled	1	Read-only	Unprotected	Unprotected

Note: X = Don't care bit.

## 5.2 Op-Code Instructions

The operations of the GT25A1024A are controlled by a set of instruction Op-Codes (Table 5.4) that are clocked-in serially via SI pin. To initiate an instruction, the chip select ( $\overline{CS}$ ) must be Low. Subsequently, each Low-to-High transition of the clock (SCK) will latch a stable level from SI. After the 8-bit Op-Code, it may continue to latch-in an address and/or data from SI accordingly, or to output data from SO. During data output, data are latched out at the falling edge of SCK. All communications start with MSB first. Upon the transmission of the last bit but prior to any following Low-to-High transition on SCK,  $\overline{CS}$  must be brought to High in order to end the transaction and start the operation. The device will enter into Standby Mode after the operation is completed.

**Table 5.4: Instruction Op-Codes [1,2,3]**

Name	Op-Code	Operation	Address	Data (SI)	Data (SO)
WREN	0000 X110	Set Write Enable Latch	-	-	-
WRDI	0000 X100	Reset Write Enable Latch	-	-	-
RDSR	0000 X101	Read Status Register	-	-	D7-D0 -
WRSR	0000 X001	Write Status Register	-	D7-D0	-
READ	0000 X011	Read Data from Array	A23-A0	-	D7-D0, ...
WRITE	0000 X010	Write Data to Array	A23-A0	D7-D0, ...	-
RDID	1000 X011	Read Identification Page	A23-A0	-	D7-D0
WRID	1000 X010	Write Identification Page	A23-A0	D7-D0	-
RDLS	1000 X011	Read the Identification Page Lock Status	A23-A0	-	-
LID	1000 X010	Lock the Identification Page	A23-A0	-	-

Notes: <sup>[1]</sup> X = Don't care bit. However, it is recommended to be "0".

<sup>[2]</sup> Some address bits may be don't care (Table 5.5).

<sup>[3]</sup> It is strongly recommended that an appropriate format of Op-Code must be entered. Otherwise, it may cause unexpected phenomenon to be occurred. Nevertheless, it is illegal to input invalid any Op-Code.

**Table 5.5: Address Key**

Address	b23	b22	b21	b20	b19	b18	b17	b16	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
WRITE or READ	x	x	x	x	x	x	x	A16	A15	A14	A13	A12	A12	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
WRID or RDID	x	x	x	x	x	x	x	x	x	x	x	x	x	0	x	x	x	A6	A5	A4	A3	A2	A1	A0





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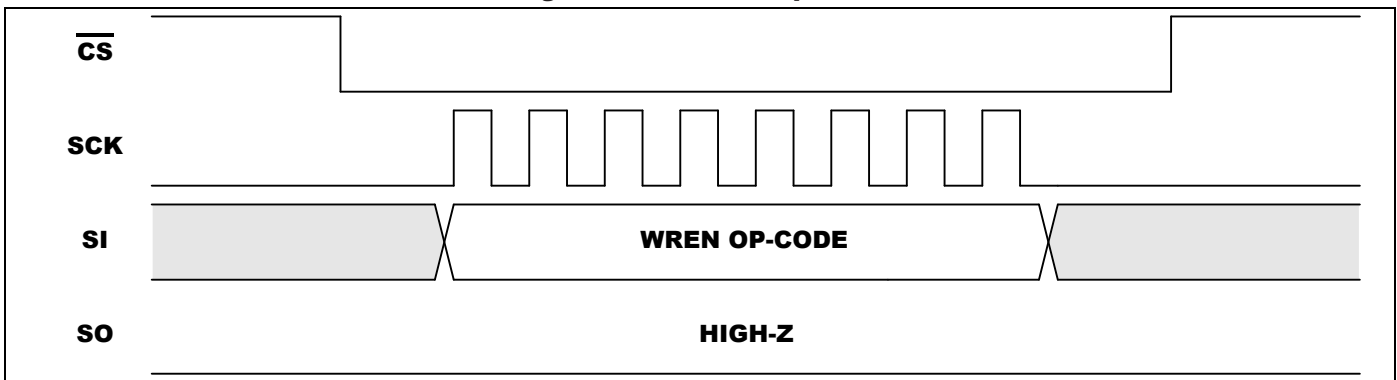
LID or RDLS	x	x	x	x	x	x	x	x	x	x	x	x	x	x	1	x	x	x	x	x	x	x	x	x	x	x	x	x
-------------	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---

Note: 'x' is don't care

### 5.3 Write Enable

When  $V_{CC}$  is initially applied, the device powers up with both status register and entire array in a write-disabled state. Upon completion of Write Disable (WRDI), Write Status Register (WRSR) or Write Data to Array (WRITE), the device resets the WEN bit in the Status Register to 0. Prior to any data modification, a Write Enable (WREN) instruction is necessary to set WEN to 1 (Figure. 5-1).

Figure 5-1. WREN Sequence

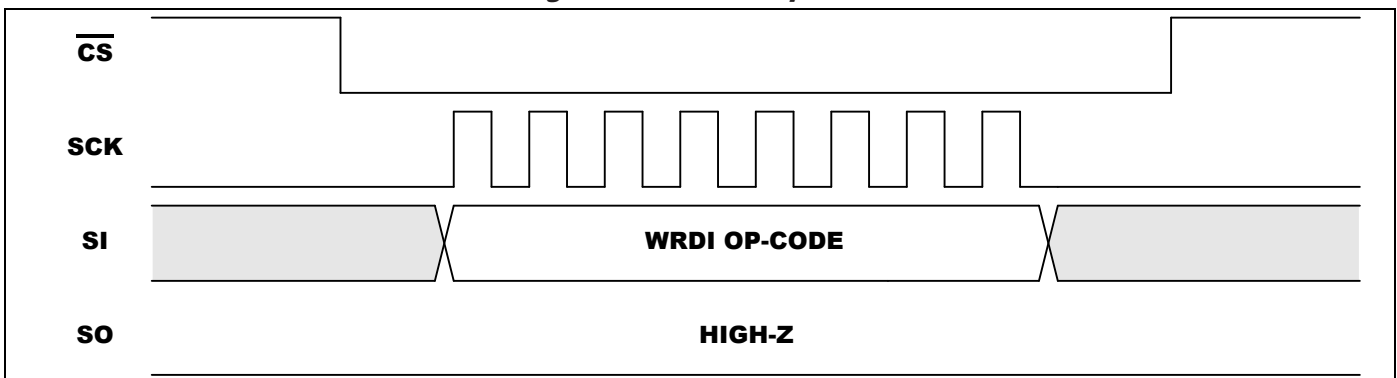


Note: Write Enable also can support 16 clock command (06XXh), XXh: don't care.

### 5.4 Write Disable

The device can be completely protected from modification by resetting WEN to 0 through the Write Disable (WRDI) instruction (Figure. 5-2).

Figure 5-2. WRDI Sequence



Note: Write Disable also can support 16 clock command (04XXh), XXh: don't care.

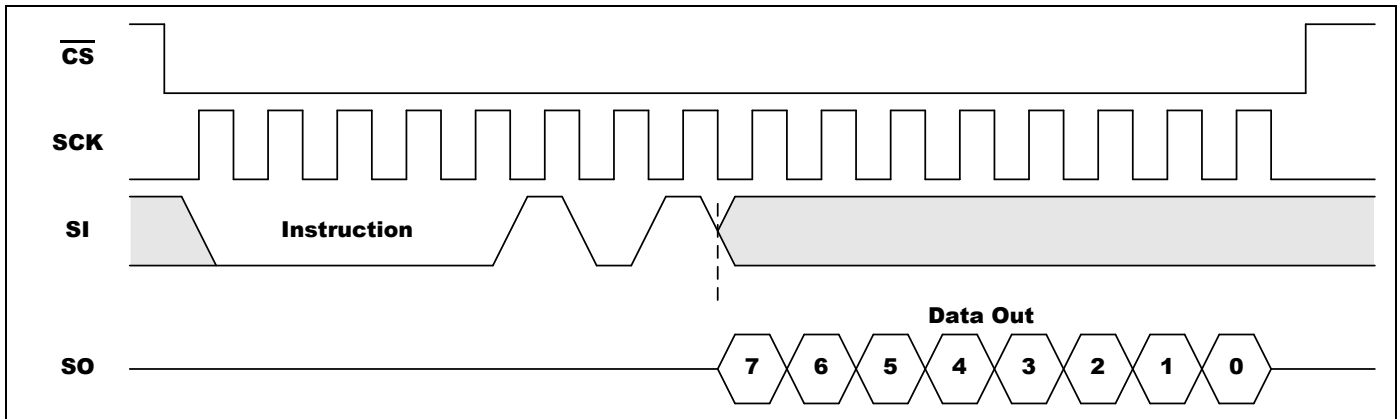
### 5.5 Read Status Register

The Read Status (RDSR) instruction reviews the status of Write Protect Enable, Block Protection setting (Table 5.2), Write Enable state and  $\overline{RDY}$  status. RDSR is the only instruction accepted when a write cycle is underway. It is recommended that the status of Write Enable and  $\overline{RDY}$  be checked, especially prior to an attempted modification of data. These 8 bits information can be repeatedly output on SO after the initial Op-Code (Figure. 5-3).



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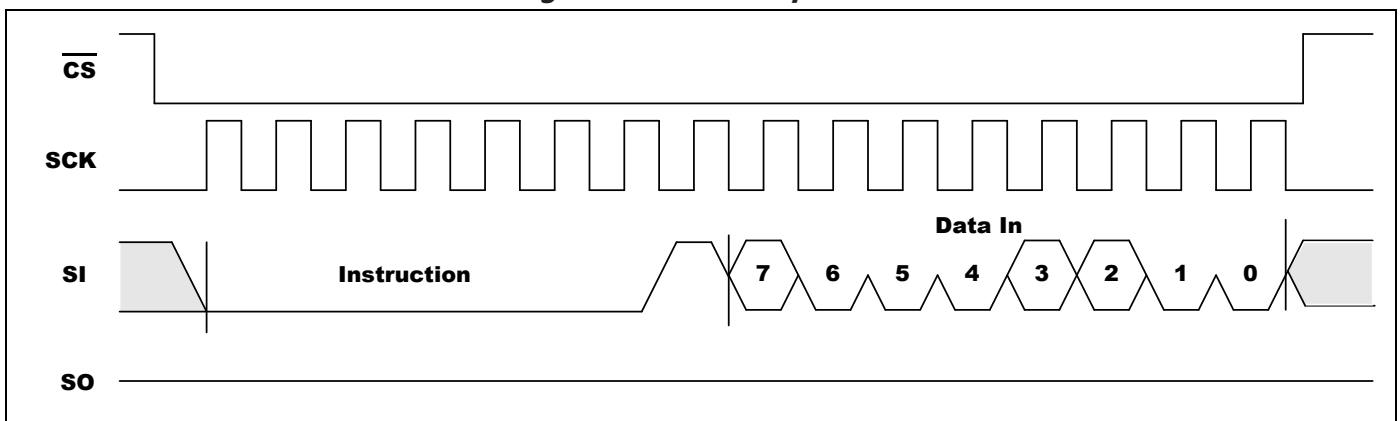
Figure 5-3. RDSR Sequence



## 5.6 Write Status Register

The Write Status Register (WRSR) instruction allows the user to choose a Block Protection setting and set or reset the WPEN bit. The values of the other data bits incorporated into WRSR can be 0 or 1 and are not stored in the Status Register. WRSR will be ignored unless both following conditions are true: a) WEN = 1, due to a prior WREN instruction; and b) Hardware Write Protection is not enabled (Table 5.3). Except for  $\overline{RDY}$  status, the values in the Status Register remain unchanged until the moment when the write cycle is completed and the register is updated. Note that WPEN can be changed from 1 to 0 only if  $\overline{WP}$  is already set High. Once completed, WEN is reset for complete chip write protection (Fig. 5-4).

Figure 5-4. WRSR Sequence



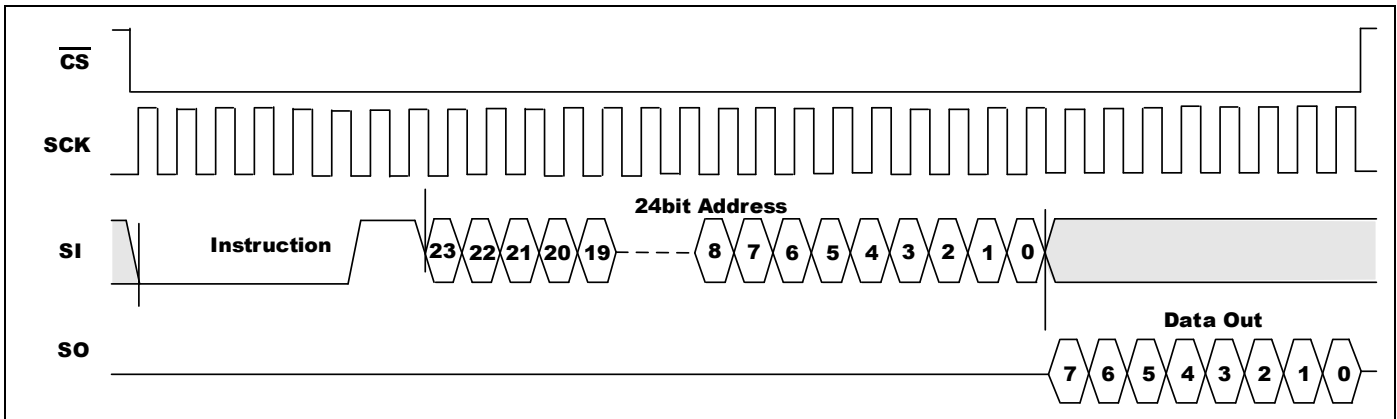
## 5.7 Read Data

This instruction includes an Op-Code and 24-bit address, then results the selected data to be shifted out from SO. Following the first data byte, additional sequential data can be output. If the data byte of the last address is initially output, then address will rollover to the first address in the array, and the output could loop indefinitely. At any time, a rising  $\overline{CS}$  signal ceases the operation (Figure. 5-5).



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Figure 5-5. READ Sequence

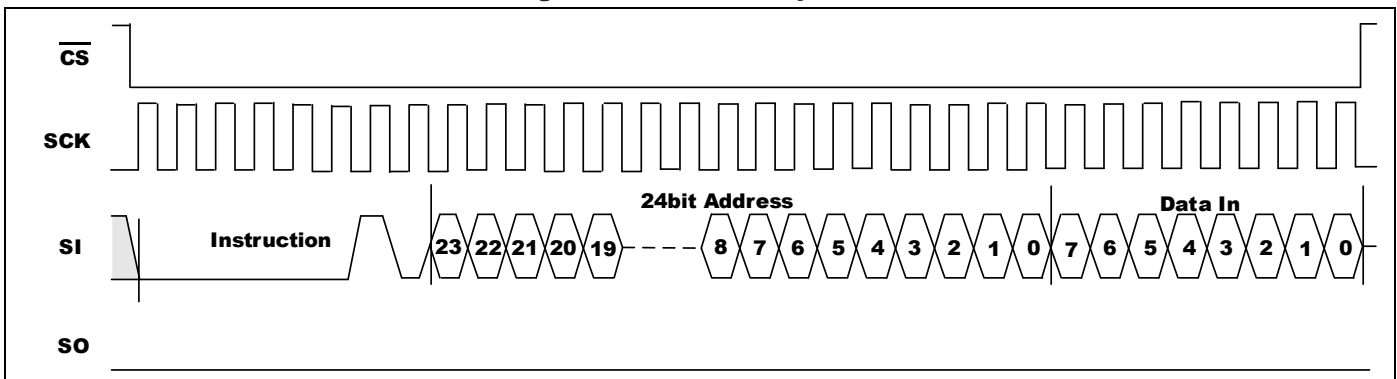


## 5.8 Write Data

The WRITE instruction contains an Op-Code, a 24-bit address and the first data byte. Additional data bytes may be supplied sequentially after the first byte. Each WRITE instruction can affect up to 256 bytes of data in a page. Each page has a starting address XXXXXXXX XXX00000 and an ending address XXXXXXXX XXX11111. After the last byte of data in a page is input, the address rolls over to the beginning of the same page. If more than 256 bytes of data is input during a single instruction, then only the last 256 bytes will be retained, but the initial data will be overwritten.

The contents of the array defined by Block Protection cannot be modified as long as that block configuration is selected. The contents of the array outside the Block Protection can only be modified if Write Enable (WEN) is set to 1. Therefore, it may be necessary that a WREN instruction is initiated prior to WRITE. Once Write operation is completed, WEN is reset for complete chip write protection (Figure. 5-6). Besides, Hardware Write Protection has no effect on the memory array.

Figure 5-6. WRITE Sequence



## 5.9 Identification Page

The GT25A1024A optionally offers an additional Identification Page (128 bytes) in addition to the 1024 Kbit memory, The Identification page contains two fields:

- Device identification: the three first byte are programmed by Giantec with the Device identification code, as shown in below Table.
- Application parameters: the bytes after the Device identification code are available for application specific data.

If the end application does not need to read the Device identification code, this field can be overwritten and used to store



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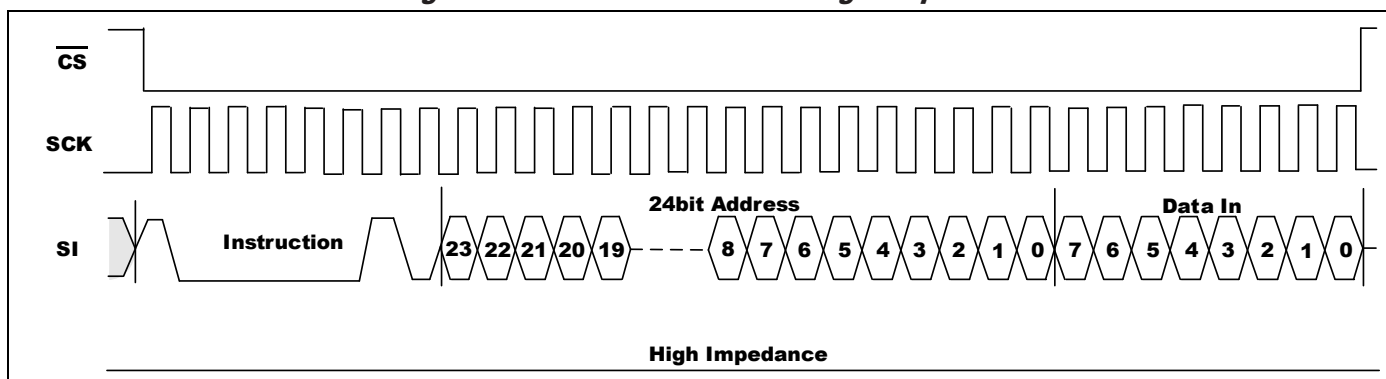
application-specific data. Once the application-specific data are written in the Identification page, the whole Identification page should be permanently locked in Read-only mode.

Address in Identification Page	Description	Value
00h	Giantec Manufacturer coder	C4h
01h	SPI Family code	00h
02h	Memory Density code	11h

## 5.9.1 Write Identification Page

The Identification Page (128 bytes) is an additional page which can be written and (later) permanently locked in Read-only mode. Writing this page is achieved with the Write Identification Page instruction (see Table 5.4), the Chip Select signal ( $\overline{CS}$ ) is first driven low. The bits of the instruction byte, address byte, and at least one data byte are then shifted in on Serial Data input (SI). Address bit A10 must be 0, address bits [A15:A11] and [A9:A7] are Don't Care, the [A6:A0] address bits define the byte address inside the identification page. The instruction sequence is shown in Figure 5-7.

Figure 5-7. Write Identification Page Sequence



## 5.9.2 Lock Identification Page

The Lock ID instruction permanently locks the Identification Page in read-only mode. Before this instruction can be accepted, a Write Enable (WREN) instruction must have been executed. The Lock ID instruction is issued by driving Chip Select ( $\overline{CS}$ ) low, sending the instruction code, the address and a data byte on Serial Data input (SI), and driving Chip Select ( $\overline{CS}$ ) high. In the address sent, A10 must be equal to 1, all other address bits are Don't Care. The data byte sent must be equal to the binary value xxxx xx1x, where x = Don't Care.

Chip Select ( $\overline{CS}$ ) must be driven high after the rising edge of Serial Clock (SCK) that latches in the eighth bit of the data byte, and before the next rising edge of Serial Clock (SCK). Otherwise, the Lock ID instruction is not executed. Driving Chip Select ( $\overline{CS}$ ) high at a byte boundary of the input data triggers the self-timed write cycle whose duration is  $T_{WR}$ . The instruction sequence is shown in Figure 5-8.

The instruction is not accepted, and so not executed, under the following conditions:

- If the Write Enable Latch (WEL) bit has not been set to 1 (by previously executing a Write Enable instruction).
- If Status register bits (BP1, BP0) = (1,1).
- If a write cycle is already in progress.



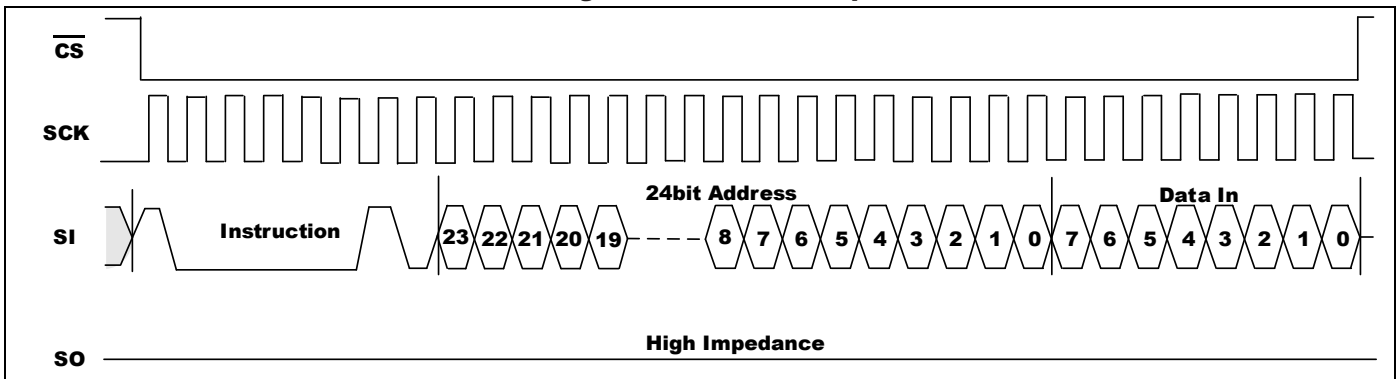
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- If the device has not been deselected, by Chip Select ( $\overline{CS}$ ) being driven high, at a byte boundary (after the eighth bit, b0, of the last data byte that was latched in).
- If the Identification page is locked by the Lock Status bit.

The Lock Identification Page instruction (Lock ID) permanently locks the Identification page in Read-only mode. The Lock ID instruction is similar to Byte Write (into memory array) with the following specific conditions:

- Address bit A10 must be '1'; all other address bits are don't care.
- The data byte must be equal to the binary value xxxx xx1x, where x is don't care.

**Figure 5-8. Lock ID Sequence**



### 5.9.3 Read Identification Page

The Identification Page (128 bytes) is an additional page which can be written and (later) permanently locked in Read-only mode. Reading this page is achieved with the Read Identification Page instruction (see Table 5.4).

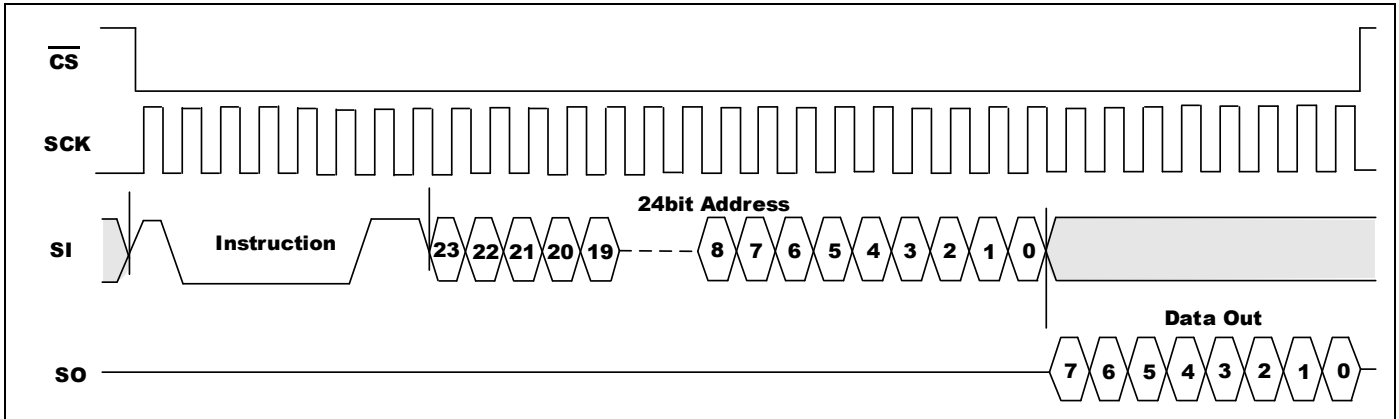
The Chip Select signal ( $\overline{CS}$ ) is first driven low, the bits of the instruction byte and address bytes are then shifted in, on Serial Data input (SI). Address bit A10 must be 0, address bits [A23:A11] and [A9:A7] are Don't Care, and the data byte pointed to by [A6:A0] is shifted out on Serial Data output (SO). If Chip Select ( $\overline{CS}$ ) continues to be driven low, the internal address register is automatically incremented, and the byte of data at the new address is shifted out.

The number of bytes to read in the ID page must not exceed the page boundary (128 bytes). There is no roll over feature in ID page. The read cycle is terminated by driving Chip Select ( $\overline{CS}$ ) high. The rising edge of the Chip Select ( $\overline{CS}$ ) signal can occur at any time during the cycle. The first byte addressed can be any byte within any page (Figure. 5-9).

The instruction is not accepted, and is not executed, if a write cycle is currently in progress.



**Figure 5-9. Read Identification Page Sequence**



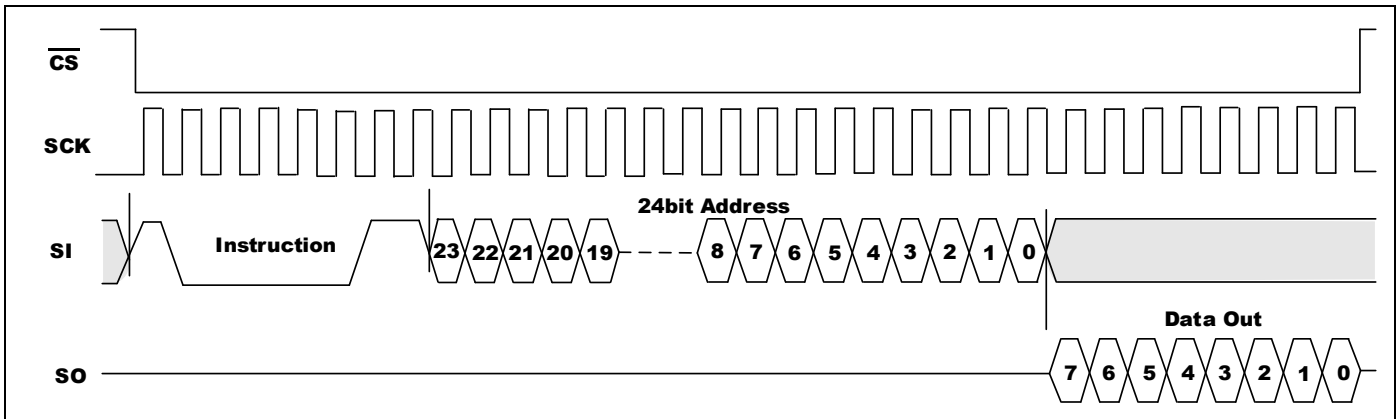
### 5.9.4 Read the lock status

The Read Lock Status instruction is used to read the lock status.

To send this instruction to the device, Chip Select (S) first has to be driven low. The bits of the instruction byte and address bytes are then shifted in (MSB first) on Serial Data input (D). Address bit A10 must be 1; all other address bits are Don't Care (it might be easier to define these bits as 0, as shown in Table 5-5). The Lock bit is the LSB (Least Significant Bit) of the byte read on Serial Data output (Q). It is at '1' when the lock is active and at '0' when the lock is not active. If Chip Select (S) continues to be driven low, the same data byte is shifted out.

The read cycle is terminated by driving Chip Select (S) high. The instruction sequence is shown in Figure 5-10

**Figure 5-10. Read Lock Status Sequence**





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## 5.10 Delivery State

GT25A1024A is shipped erased status with all bytes value as FFh.

## 6. Application Recommendation

### 6.1 Operating Supply Voltage

Prior to selecting the memory and issuing instructions to it, a valid and stable VCC voltage within the specified [VCC(min), VCC(max)] range must be applied. This voltage must remain stable and valid until the end of the transmission of the instruction and, for a Write instruction, until the completion of the internal Write cycle (tW).

In order to filter out small ripples on VCC, it is recommended to connect a decoupling capacitor (typically 0.1 μf) between VCC and GND.

### 6.2 Power-up conditions

During power ramp up, once VCC level reaches the power on reset threshold, the EEPROM internal logic is reset to a known state. While VCC reaches the stable level above the minimum operation voltage, the EEPROM can be operated properly.

Therefore, in a good power on reset, VCC should always begin at 0V and rise straight to its normal operating level, instead of being at an uncertain level. Only after a good power on reset, can EEPROM work normally.

At power-up, the device does not respond to any instruction until VCC reaches the internal threshold voltage (this threshold is defined in the DC characteristic Table as V<sub>RES</sub>).

When VCC passes over the POR threshold, the device is reset and in the following state:

- in the Standby power mode
- deselected

As soon as the VCC voltage has reached a stable value within the [VCC(min), VCC(max)] range, the device is ready for operation.

### 6.3 Power-down

During power-down (continuous decrease in the VCC supply voltage below the minimum VCC operating voltage), the device must be in Standby power mode (that is after a STOP condition or after the completion of the Write cycle tW if an internal Write cycle is in progress).

### 6.4 ECC (Error Correction Code) and Write cycling

The Error Correction Code (ECC) is an internal logic function which is transparent for the SPI communication protocol.

The ECC logic is implemented on each group of four EEPROM bytes <sup>[1]</sup>. Inside a group, if a single bit out of the four bytes happens to be erroneous during a Read operation, the ECC detects this bit and replaces it with the correct value. The read reliability is therefore much improved.

Even if the ECC function is performed on groups of four bytes, a single byte can be written independently. In this case, the ECC function also writes the three other bytes located in the same group <sup>[1]</sup>. As a consequence, the maximum cycling budget is defined at group level and the cycling can be distributed over the 4 bytes of the group: the sum of the cycles seen by byte0, byte1, byte2 and byte3 of the same group must remain below the maximum value defined in 7.4 Reliability.

Note: 1. A group of four bytes is located at addresses [4\*N, 4\*N+1, 4\*N+2, 4\*N+3], where N is an integer.



# GT25A1024A

## 7. Electrical Characteristics

### 7.1 Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V <sub>S</sub>	Supply Voltage	-0.5 to V <sub>CC</sub> + 1	V
V <sub>P</sub>	Voltage on Any Pin	-0.5 to V <sub>CC</sub> + 1	V
T <sub>STG</sub>	Storage Temperature	-65 to +150	°C
I <sub>OUT</sub>	Output Current	5	mA
V <sub>ESD</sub>	Electrostatic pulse (Human Body model)	±8000	V

Note: Stress greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

### 7.2 Operating Range

Range	Ambient Temperature (T <sub>A</sub> )	V <sub>CC</sub>
Automotive Grade 1	-40°C to +125°C	1.7V to 5.5V

### 7.3 Capacitance

Symbol	Parameter <sup>[1, 2]</sup>	Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	-	6	pF
C <sub>I/O</sub>	Input / Output Capacitance	-	8	pF

Notes: <sup>[1]</sup> Tested initially and after any design or process changes that may affect these parameters and not 100% tested.

<sup>[2]</sup> Test conditions: T<sub>A</sub> = 25°C, f = 1 MHz, V<sub>CC</sub> = 5.0V.

### 7.4 Reliability

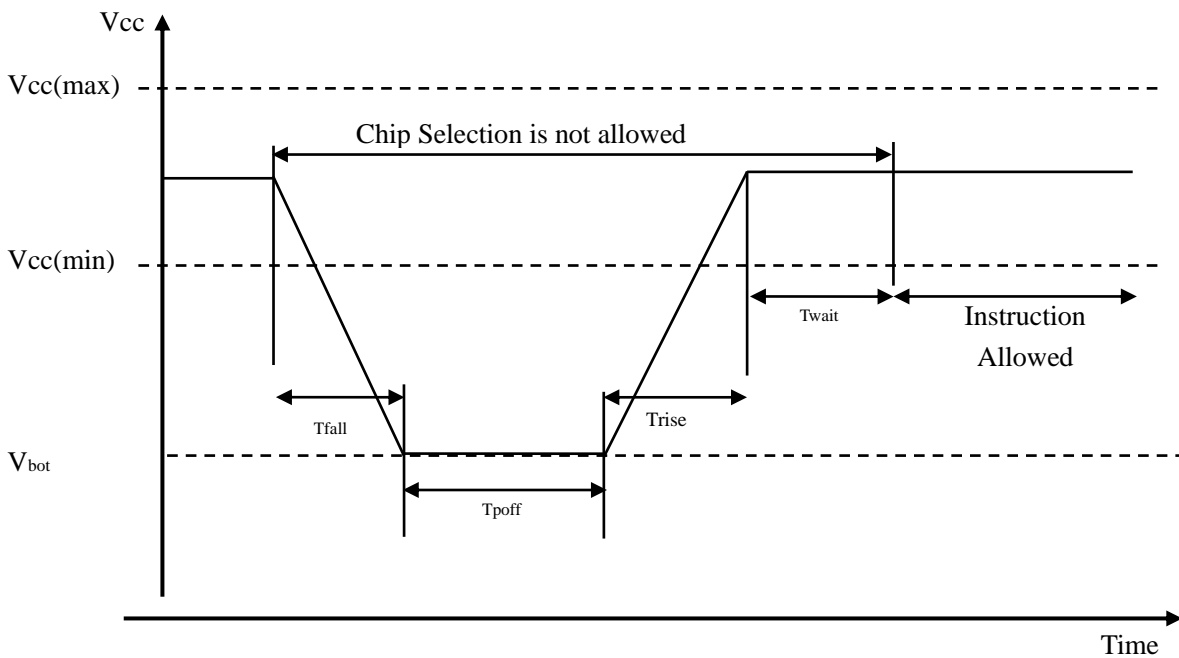
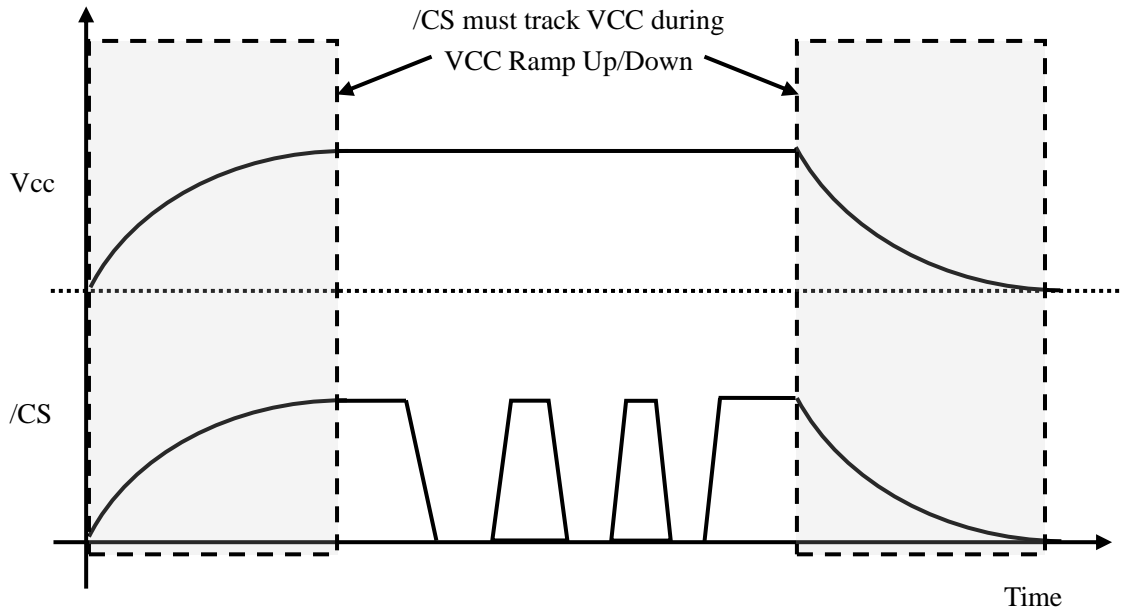
Symbol	Parameter	Condition	Min.	Unit
End	Endurance	T <sub>a</sub> =+25°C	4 million	Program / Erase Cycles
		T <sub>a</sub> =+85°C	1.2 million	
		T <sub>a</sub> =+125°C	600 k	
DR	Data Retention	T <sub>a</sub> =+25°C	100	Years
		T <sub>a</sub> =+125°C	50	





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## 7.5 Power Up/Down and Voltage Drop



Power down-up Timing



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Symbol	Parameter	min	max	unit
V <sub>bot</sub>	VCC at power off		0.2	V
T <sub>fall</sub>	VCC min to Vbot	1		ms
T <sub>poff</sub>	VCC at power off time	100		ms
Trise	Vbot to VCC min		1	ms
Twait	VCC Min to Instruction	500		us

\* All parameters may be changed after the design or process change.

## 7.6 DC Electrical Characteristic

Symbol	Parameter	V <sub>CC</sub>	Test Conditions	Min.	Max.	Unit
V <sub>CC</sub>	Supply Voltage			1.7	5.5	V
V <sub>IH</sub>	Input High Voltage			0.7* V <sub>CC</sub>	V <sub>CC</sub> +0.5	V
V <sub>IL</sub>	Input Low Voltage			-0.3	0.3* V <sub>CC</sub>	V
I <sub>LI</sub>	Input Leakage Current		V <sub>IN</sub> = 0V To V <sub>CC</sub>	-2	2	μA
I <sub>LO</sub>	Output Leakage Current		V <sub>OUT</sub> = 0V To V <sub>CC</sub> , $\overline{CS}$ = V <sub>CC</sub>	-3	3	μA
V <sub>OH</sub>	Output High Voltage	1.7	I <sub>OH</sub> = -0.1mA	0.8*V <sub>CC</sub>	—	V
		2.5	I <sub>OH</sub> = -0.4mA	0.8*V <sub>CC</sub>	—	V
		5	I <sub>OH</sub> = -2 mA	0.8*V <sub>CC</sub>	—	V
V <sub>OL</sub>	Output Low Voltage	1.7	I <sub>OL</sub> = 0.15 mA	—	0.2	V
		2.5	I <sub>OL</sub> = 1.5 mA	—	0.4	V
		5	I <sub>OL</sub> = 2 mA	—	0.4	V
I <sub>CC1</sub>	Operating Current	1.7	Read at 5 MHz, SO=Open	—	2	mA
		2.5	Read at 10 MHz, SO=Open	—	4	mA
		5	Read at 20 MHz, SO=Open	—	5	mA
I <sub>CC2</sub>	Operating Current	1.7	Write at 5 MHz, SO=Open	—	2	mA
		2.5	Write at 10 MHz, SO=Open	—	2	mA
		5	Write at 20 MHz, SO=Open	—	2	mA
I <sub>SB</sub>	Standby Current	1.7	V <sub>IN</sub> = V <sub>CC</sub> or GND, $\overline{CS}$ = V <sub>CC</sub>	—	3	μA
		2.5	V <sub>IN</sub> = V <sub>CC</sub> or GND, $\overline{CS}$ = V <sub>CC</sub>	—	5	μA
		5	V <sub>IN</sub> = V <sub>CC</sub> or GND, $\overline{CS}$ = V <sub>CC</sub>	—	10	μA



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## 7.7 AC Electrical Characteristic

Symbol	Parameter <sup>[1]</sup>	1.7V ≤ V <sub>CC</sub> < 2.5V		2.5V ≤ V <sub>CC</sub> < 4.5V		4.5V ≤ V <sub>CC</sub> ≤ 5.5V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
F <sub>SCK</sub>	SCK Clock Frequency	0	5	0	10	0	20	MHz
T <sub>RI</sub>	Input Rise Time	—	1	—	1	—	1	μs
T <sub>FI</sub>	Input Fall Time	—	1	—	1	—	1	μs
T <sub>WH</sub>	SCK High Time	80	—	40	—	20	—	ns
T <sub>WL</sub>	SCK Low Time	80	—	40	—	20	—	ns
T <sub>CS</sub>	$\overline{\text{CS}}$ High Time	100	—	50	—	25	—	ns
T <sub>CSS</sub>	$\overline{\text{CS}}$ Setup Time	100	—	50	—	25	—	ns
T <sub>CSH</sub>	$\overline{\text{CS}}$ Hold Time	100	—	50	—	25	—	ns
T <sub>SU</sub>	Data In Setup Time	20	—	10	—	5	—	ns
T <sub>H</sub>	Data In Hold Time	20	—	10	—	5	—	ns
T <sub>HD</sub>	$\overline{\text{HOLD}}$ Setup Time	20	—	10	—	5	—	ns
T <sub>CD</sub>	$\overline{\text{HOLD}}$ Hold Time	20	—	10	—	5	—	ns
T <sub>V</sub> <sup>[2]</sup>	Output Valid	0	80	0	40	0	20	ns
T <sub>HO</sub>	Output Hold Time	0	—	0	—	0	—	ns
T <sub>LZ</sub>	$\overline{\text{HOLD}}$ to Output Low Z	0	80	0	40	0	25	ns
T <sub>HZ</sub>	$\overline{\text{HOLD}}$ to Output High Z	—	80	—	40	—	40	ns
T <sub>DIS</sub>	Output Disable Time	—	80	—	40	—	40	ns
T <sub>WC</sub>	Write Cycle Time	—	5	—	5	—	5	ms

Notes: <sup>[1]</sup> The parameters are characterized but not 100% tested.

<sup>[2]</sup>C<sub>L</sub> = 30pF (typical)



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## 7.8 Timing Diagrams

Figure 7-1. Synchronous Data Timing

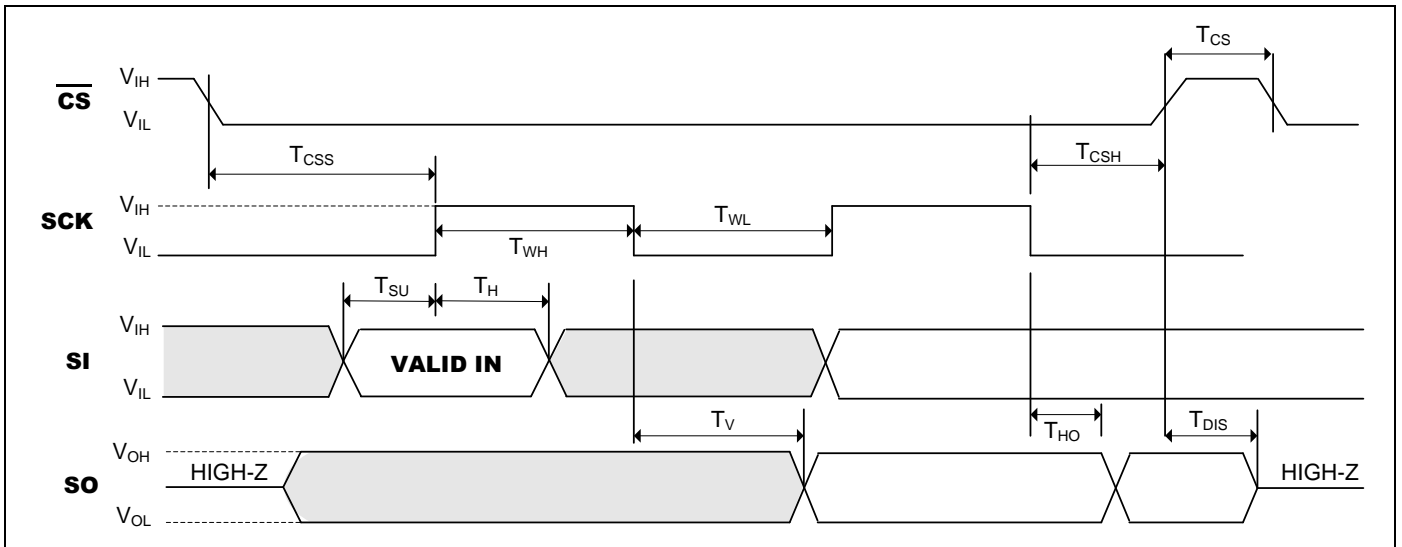
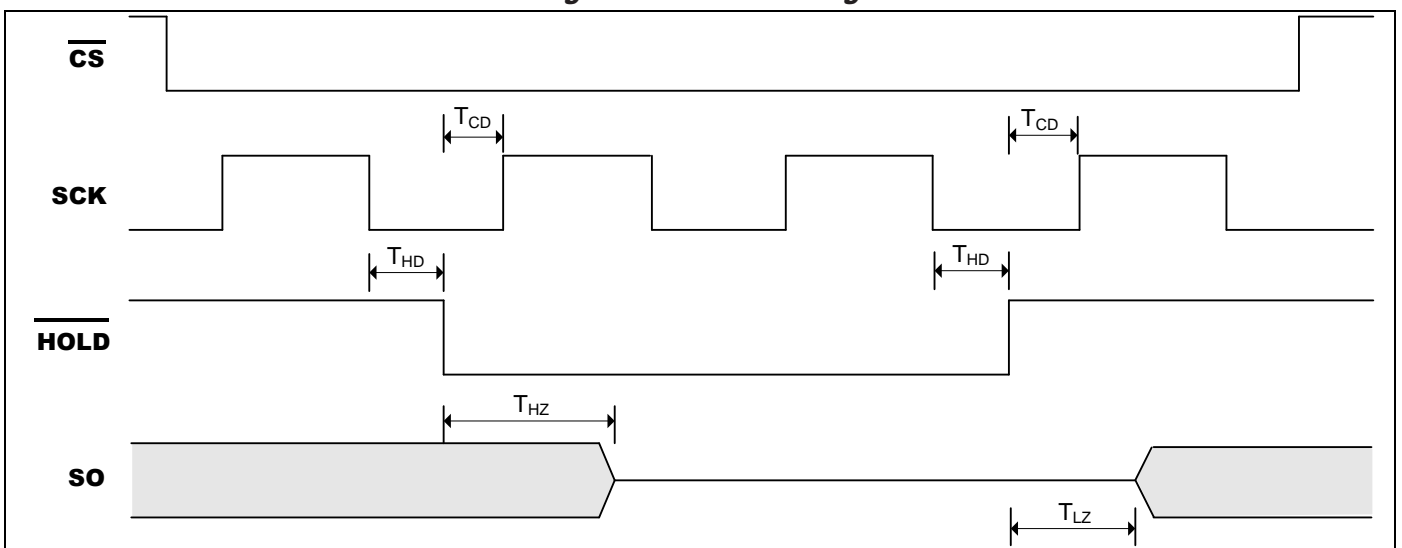


Figure 7-2. HOLD Timing





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## 8. Ordering Information

Voltage Range	Part Number*	Package (8-pin)*
1.7V to 5.5V	GT25A1024A-2GLA1-TR	150-mil SOIC
	GT25A1024A-2ZLA1-TR	3 x 4.4 mm TSSOP

### Rule:

<b>Device Type</b> GT25A = SPI Protocol Automotive EEPROM
<b>Device Density</b> 1024A = 1024K-bit Product version A
<b>Operating Voltage</b> 2 = 1.7/1.8-5.5V 3 = 2.3/2.5-5.5V
<b>Package</b> G = SOP8 150mil Z = TSSOP8
<b>Pb Status</b> L = green status (HF, Meet reach, Rohs, etc.)
<b>Temperature Range</b> A1 = Automotive Grade1 (-40C ~ +125°C) A2 = Automotive Grade2 (-40C ~ +105°C)
<b>Packing</b> TR = Tape & Reel

### Note:

1. Contact Giantec Sales Representatives for availability and other package information.
2. The product is packed in tape and reel "-TR" (4K per reel).
3. Refer to Giantec website for related declaration document on lead free, RoHS, halogen free or Green, whichever is applicable.

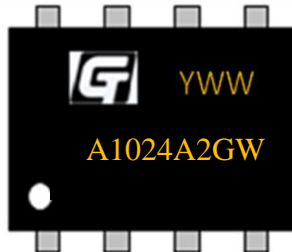


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## 9. Top Markings

### 9.1 SOIC Package

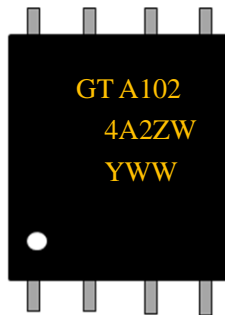


**G:** Giantec Logo

A1024A2GW: GT25A1024A-2GLA1-TR

YWW: Date Code, Y=year, WW=week

### 9.2 TSSOP Package



**GT:** Giantec Logo

A102 4A2ZW: GT25A1024A-2ZLA1-TR

YWW: Date Code, Y=year, WW=week

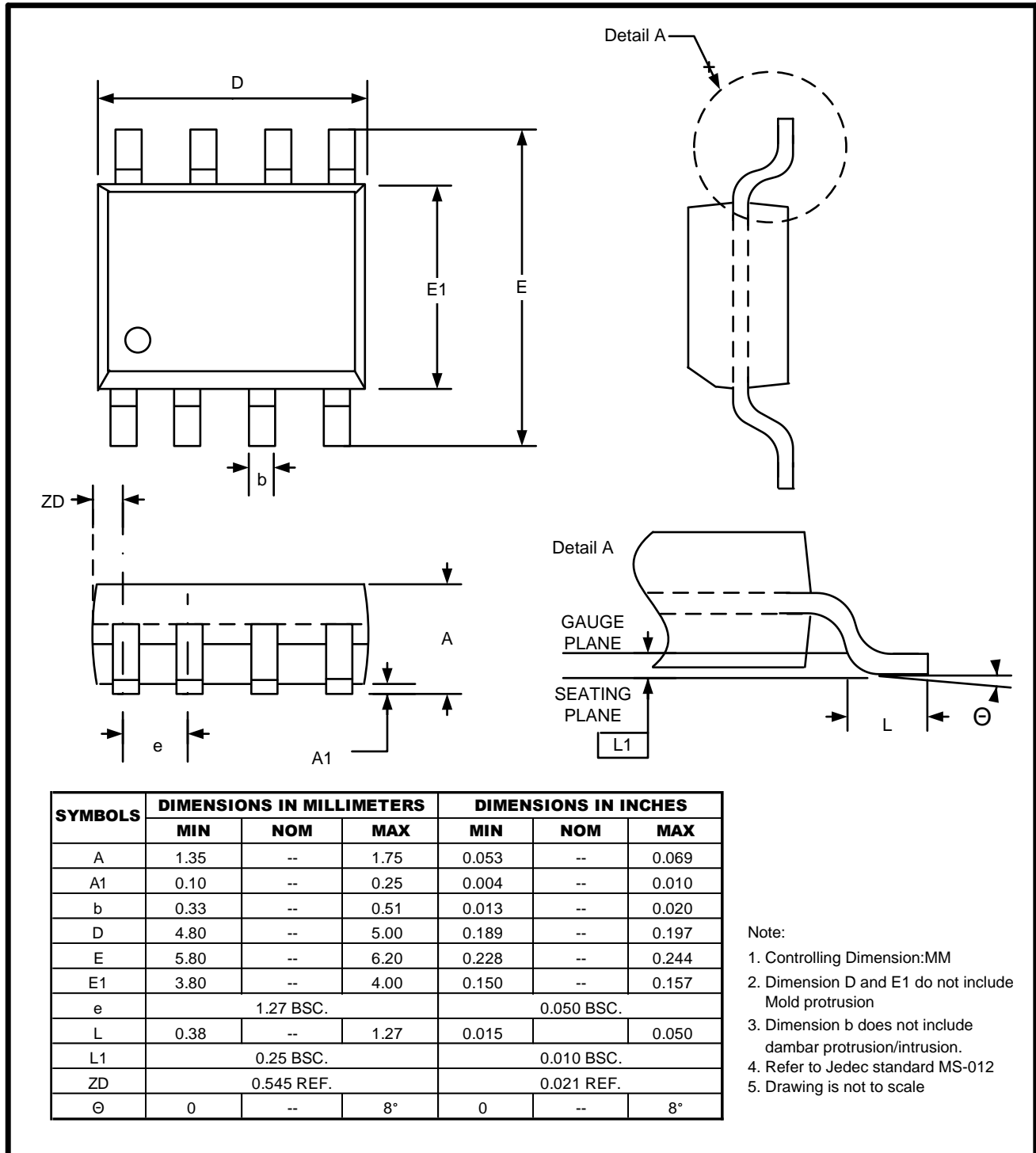


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## 10. Package Information

### 10.1 SOP

#### 8L 150mil SOIC Package Outline

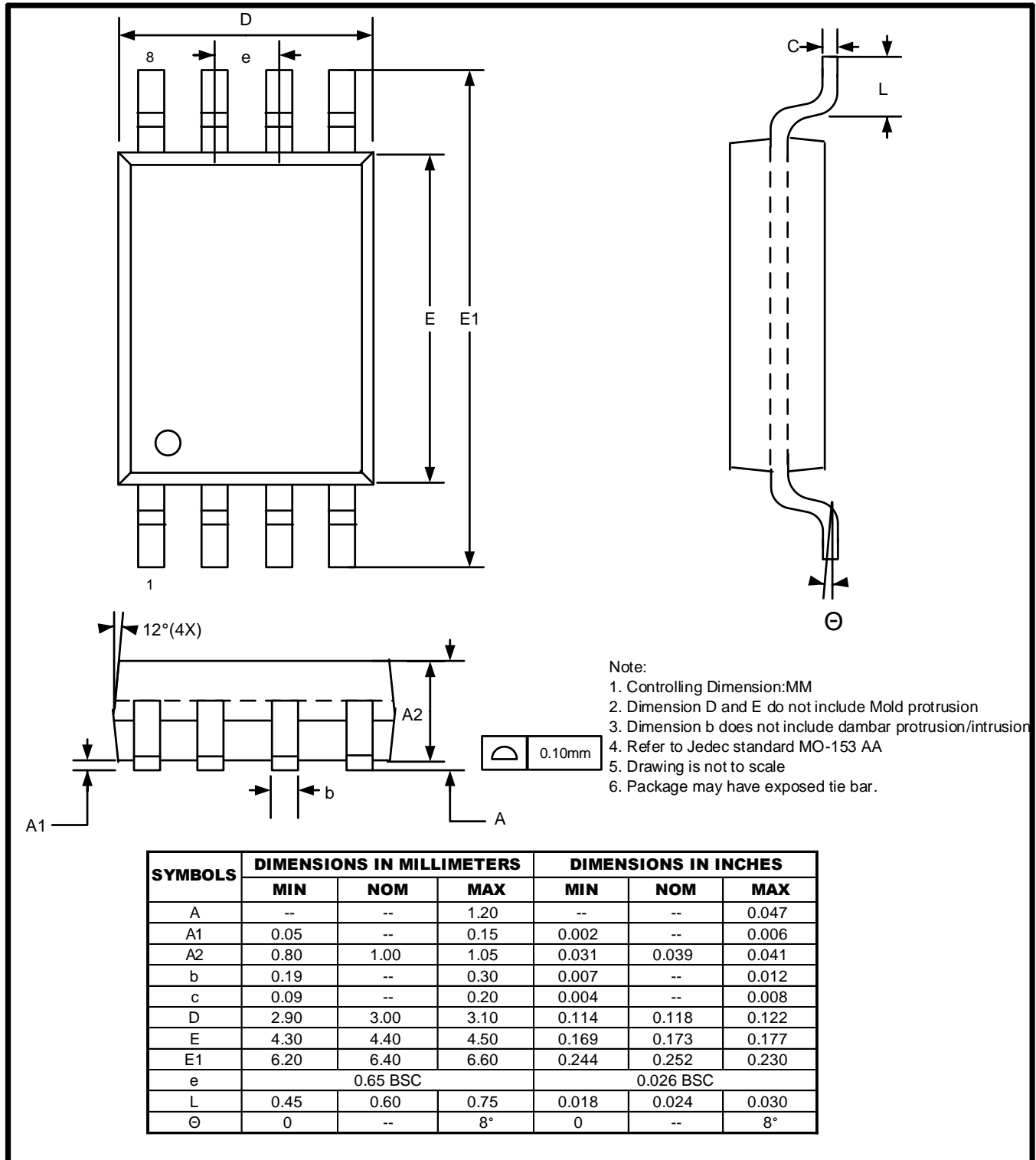




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## 10.2 TSSOP

### 8L 3x4.4mm TSSOP Package Outline







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## 11. Revision History

Revision	Date	Descriptions
1.0	NOV.2020	Initial Version
1.1	May. 2022	Update Logo and other
1.2	Jun. 2022	Update ISB Spec
1.3	Aug. 2022	Add note for $\overline{WP}$ in <b>4.3</b>
1.4	Mar. 2023	Update ILO,ISB
1.5	Mar. 2023	Add note for <b>HOLD</b> in 4.3, delete note for $\overline{WP}$ in <b>4.3</b>
1.6	Aug.2024	Add some notes in Table 5.1